DATA SHEET

Revision: 1.2

Release date: 17/12/2018

RDA16110E

Fully Integrated, Direct Down-Conversion Satellite Receiver for DVB-S, DVB-S2 & ABS-S, MMDS

Update History

Rev	Date	Author	History Description
1.0	2015-3-3	Peng Xiaofei	The primary edition
1.1	2015-12-15	Peng Xiaofei	Final edition
1.2	2018-12-17	Choo MC	Amend upper Frequency range from 2350MHz to 2320MHz

1. General Description

RDA16110E is a fully-integrated direct-conversion RF front end for digital satellite reception standards, such as DVB-S, DVB-S2, ABS-S and MMDS. The receiving frequency range is from 250MHz to 2320MHz, and the baseband filter's bandwidth can be selected from 4MHz to 40MHz by 1MHz step.

RDA16110E consists of a variable gain LNA, quadrature down-converter, variable IF gain amplifiers, variable low-pass filters, reference oscillator, VCOs, synthesizer and output baseband amplifier to drive external ADC.

Based on RDA's some innovative technique, the RDA16110E offers excellent phase noise and very low implementation loss, required for advanced modulation systems such as 8PSK and DVB-S2. This tuner RF IC does not require a balun and its fully integrated design saves valuable board space and simplifies RF layout.

1.1. Features

- Single-chip RF-to-baseband Satellite receiver
- CMOS Fully integrated RF front end
- Low noise and wide dynamic range zero-IF receiver
- Input frequency range: 250 to 2320 MHz
- Input signal level: -100 to 5dBm
- More than 85dB gain control range
- Fully integrated PLL (dividers, charge pump, phase & frequency detectors, loop filters, etc.)
- Integrated RX VCO
- Integrated baseband LPF with selectable cut-off frequency from 4MHz to 40MHz by 1MHz step
- Integrated LNA with RF AGC
- Integrated reference oscillator (27MHz is default)
- I^2C bus interface
- Automatic gain control
- 0.11μm RF CMOS technology
- 3V to 3.6V operation
- Power consumption of less than 600mW
- Lower profile packages: 4×4 mm QFN24

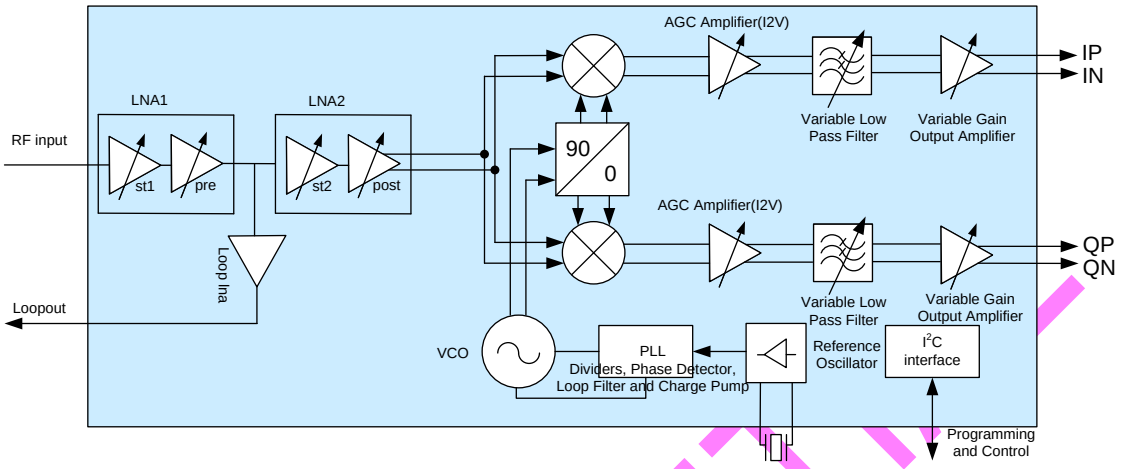
1.2. Applications

- Set-top boxes
- Digital video recorders
- Digital television
- Satellite PC-TV

- SMATV trans-modulators (Satellite Master Antenna TV)

2. Table of Contents

3. Functional Block Diagram



4. Functional Description

The loop LNA is used to generate the loopout signal. LNA1&LNA2 are on-chip variable gain LNAs in order to provide a wide tuner dynamic range. A direct conversion architecture is used to convert the RF signal to in-phase and quadrature baseband signals. The signals required for direct conversion are all generated within the chip by a fully integrated PLL and a quadrature LO generator. The frequency of the VCO is set by internal PLL circuits, which are programmable via a 2-wire (I2C) serial bus. The LO signals are mixed with the RF signal input and then filtered by low-pass filters to remove the upper image production by the mixer. A variable gain amplifier is then used to adjust the baseband signal levels before processing by the channel-select filters to optimize noise performance and prevent distortion within the filters. The channel-select filters are digitally programmable low pass filters with 1MHz step from 4MHz to 40MHz. The output amplifiers buffer the signal from the filters to increase the driving capability to the next baseband ADC.

Some innovative techniques are used to correct and alleviate DC offsets inherent in direct conversion mixers, the channel -select filters and output buffers.

Loop LNA

The loopout LNA is used to generate the loopout signal.

LNA1&LNA2

LNA1 is the first LNA and receives a signal from the LNB through an external matching circuit, whose input resistance is matched to 75Ω coaxial cable. The LNA2 is the second LNA and is used to provide wide dynamic range, better noise figure. The gain both of LNA1 and LNA2 can be programmed with the 2-wire (I2C) interface to insure wide dynamic range of the receiver.

AGC Amplifier

The AGC Amplifier receives the IQ signals from the quadrature mixer then amplifies them and sends to the baseband low pass filter. The gain is also programmed and controlled by the 2-wire (I2C) interface.

Baseband LPF

The baseband low-pass filter is designed to have variable cut-off frequency. The bandwidth of the LPF is selectable from 4MHz to 40MHz with 1MHz step. The DC-offset calibration can be carried out controlled by the interface. An innovative technique ensures the filter's bandwidth variety within 5%.

Reference Oscillator

The oscillator is on-chip integrated and both crystal and crystal oscillator are supported. The 27MHz is default recommended. The centre oscillation frequency can be adjusted accurately with the XAFC pin (optional function).

VCO

The receiver integrates two VCOs which ensure covering the full receiving frequency from 250MHz to 2320MHz. The two VCOs can be switched between each other selected by relevant registers and the VCO's band is programmed using the 2-wire (I2C) interface. The first VCO oscillates from 3980MHz to 6290MHz, the second from 6000MHz to 9500MHz. After divided by four, eight or sixteen, LO signal from 250(4000/16)MHz to 2320(9280/4) can be obtained.

LO frequency	Used VCO	Divider	Note
250(4000/16) ≤F≤388(6208/16)	VCO1	16	**VCO1** oscillates from 3980MHz to 6290MHz. **VCO2** oscillates from 6000MHz to 9400MHz
389(6224/16) ≤F≤537(8592/16)	VCO2	16	
538(4304/8) ≤F≤776(6208/8)	VCO1	8	
777(6216/8)≤F≤1075(8600/8)	VCO2	8	
1076(4304/4)≤F≤1552(6208/4)	VCO1	4	
1553(6212/4)≤F≤2320(9280/4)	VCO2	4	

PLL

The fractional-N frequency synthesizer uses 27MHz reference as default. The dividers, loop filters, phase & frequency detector, charge pump are all integrated on chip.

Baseband Output Amplifier

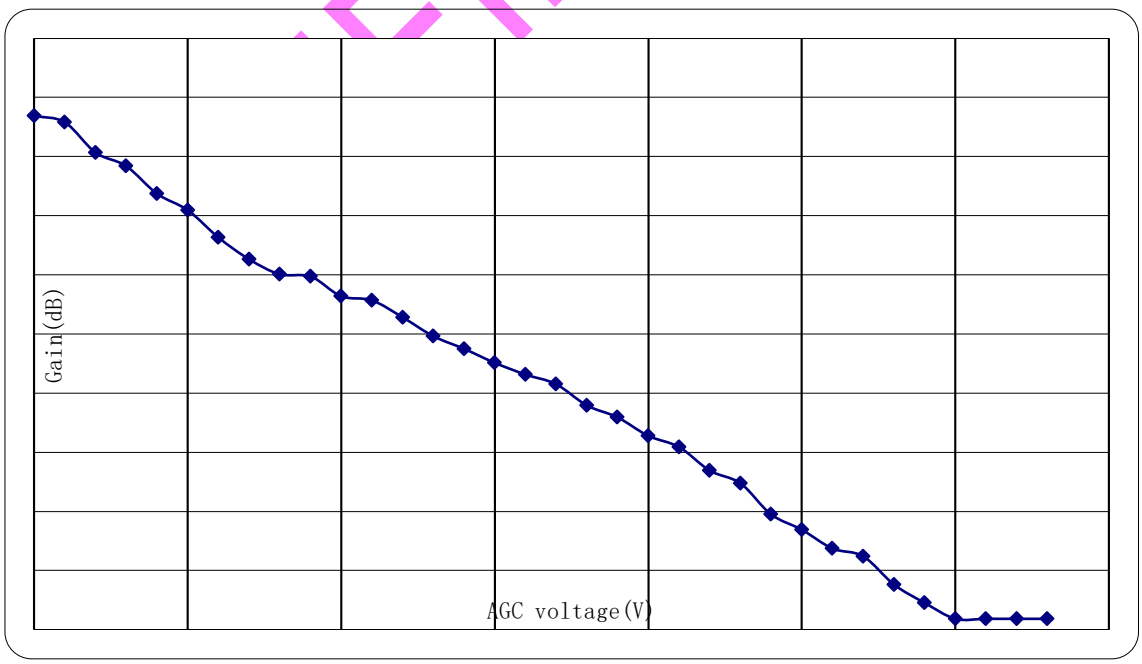
Class-AB architecture is selected for the output buffer, this makes it more flexible to the next baseband solution's input load. The gain of this stage can also be programmed with the interface to further increase the receiver dynamic.

I2C interface

The interface is the control unit of all the analog blocks, it is provided for configuration and monitoring all internal registers. The I2C bus consists of two wires: serial clock line (SCL) and serial data line (SDA). LNA's gain, AGC, baseband LPF's bandwidth, VCO's and crystal oscillator's current, VCO's oscillation frequency are all controlled by the 2-wire interface.

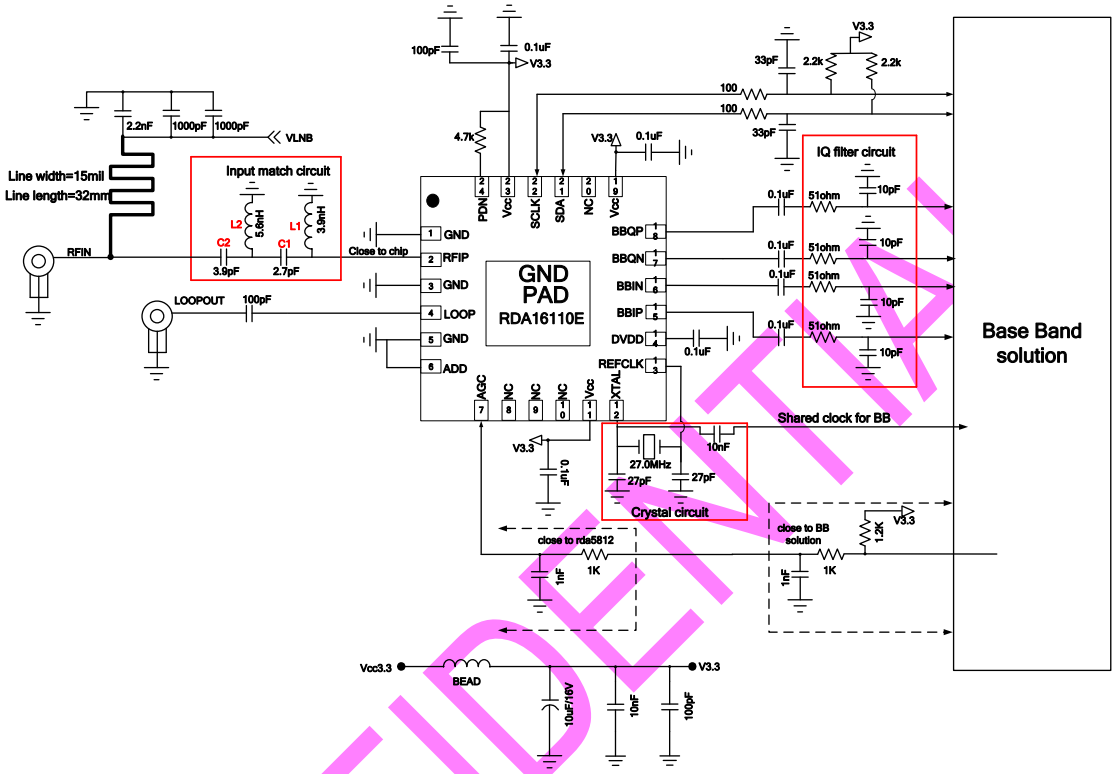
Direct AGC control

Through the AGC pin input, the receiver chain's gain can be directly controlled by the baseband solutions. The receiver gain changes inversely with the AGC control signal, this means that when AGC signal goes high, the receiver gain will reversely drop to relevant level.



5. Typical application circuit

Application circuit 1 (for DVB-S/S2 950M~2320M)



Note:

1. The input match circuit

This circuit is OPTIONAL for better S11,

With input match circuit	Without input match circuit	Note
C1=2.7pF,C2=3.9pF L1=3.9nH,L2=5.6nH	C1=0ohm, C2=0ohm L1=NC, L2=NC	L1&L2 must be high frequency inductor and self-resonant frequency must greater than 3GHz

2. IQ filter circuit

This circuit is OPTIONAL.

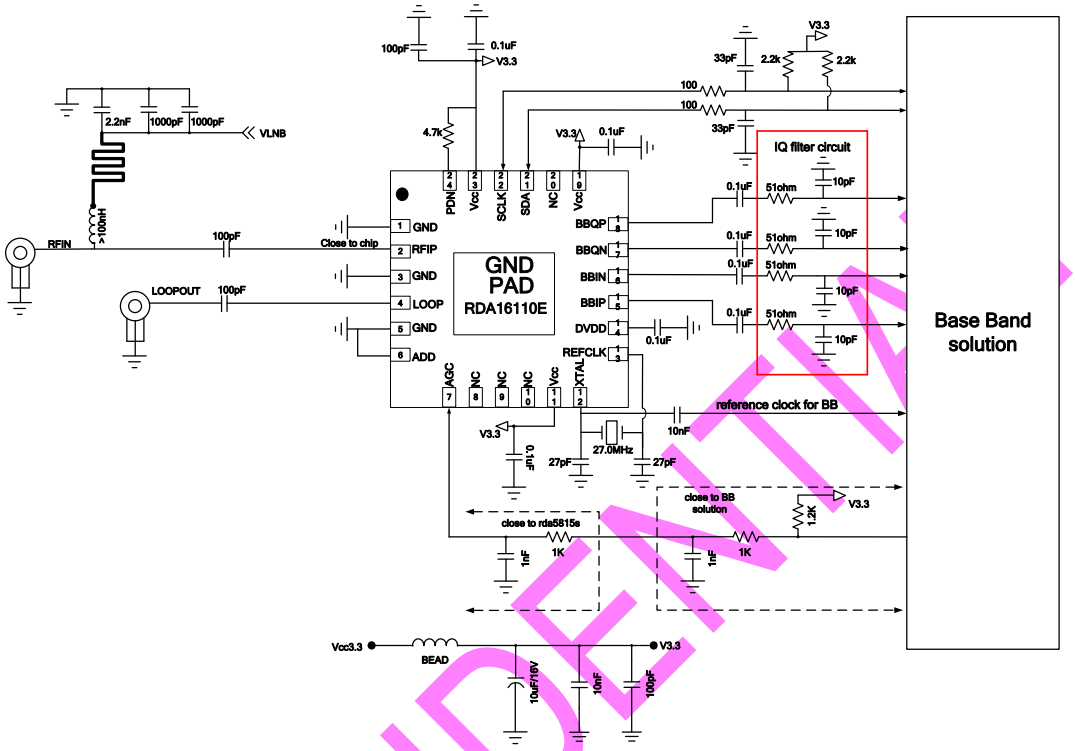
Whether this circuit is used or not according to the test result adatpted to different demodulator chip and PCB.

3. Crystal circuit

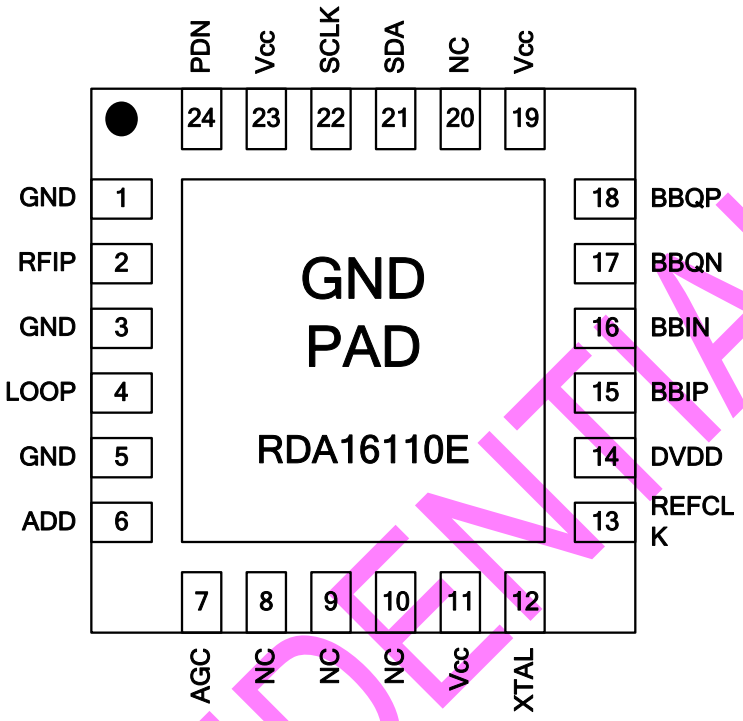
The value of load capacitance is determined by the crystal parameter.

The shared clock is OPTIONAL according to the solution requirement.

Application circuit 2 (for 250M~2320M)



6. Pin Description



Pin number	Name	I/O	DESCRIPTION
1	GND		GND
2	RFIP	I	RF Positive Input
3	GND		GND
4	LOOP	O	LOOPOUT
5	GND		GND
6	ADD	I	I2C bus address selection terminal. Allowing the use of more than one device per I2C bus system by the voltage on this pin. Refer to table 8 for programming details.
7	AGC	I	AGC control input from baseband solutions
8	NC		Not connected.
9	NC		Not connected.
10	NC		Not connected.
11	Vcc	I	Supply voltage for 16110E. Connected to 3.3 V..
12	XTAL	I/O	Connect to Crystal (27MHz is recommended)
13	REFCLK	I/O	Connect to Crystal (if using external crystal oscillator, this pin connect to the oscillator's output)
14	DVDD	O	Output of the supply voltage for Digital, Connected to cap

15	BBIP	O	Baseband positive I output
16	BBIN	O	Baseband negative I output
17	BBQN	O	Baseband negative Q output
Pin number	**Name**	**I/O**	**DESCRIPTION**
18	BBQP	O	Baseband positive Q output
19	Vcc	I	Supply voltage for 16110E. Connected to 3.3 V.
20	NC		Not connected.
21	SDA	I/O	Serial data input/output, connected to 3.3V with 10kΩ resistor
22	SCLK	I	Serial clock input
23	Vcc	I	Supply voltage for 16110E. Connected to 3.3 V.
24	PDN	I	Receiver power control If LOW, chip powered down, including the crystal oscillator. If HIGH, chip be enabled.

7. Electrical Specifications

Table 7-1. Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	AVDD	3	3.3	+3.6	V
Ambient Temperature	T_A	-25	27	+85	℃

Table 7-2. DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V_{IL}	0		0.3*VDD	V
CMOS High Level Input Voltage	V_{IH}	0.7*VDD		VDD	V
CMOS Threshold Voltage	V_{TH}		0.5*VDD		V

Table 7-3. Power Consumption Specification

(VDD =3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
ICC	Receiver on			170	175	mA
ICC(standby)	tuner Disabled	PDN=1,Enable=0,Rxon=0		6	7	mA

Table 7-4. System Characteristics

(VDD = 3 to 3.6 V, TA = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	F_{IN}		250		2320	MHz
Minimum RF input	RFIL	4.42MS/s, QPSK3/4,noise free		-97	-95	dBm
Maximum RF input	RFIH	4.42MS/s, QPSK3/4, noise free		5		dBm
Minimum RF input	RFIL	45MS/s, QPSK3/4, noise free		-87	-85	dBm
Maximum RF input	RFIH	45MS/s, QPSK3/4, noise free		5		dBm
Parameter	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Noise Figure	NF	Max Gain (Minimum AGC)		3.0	5.5	dB
Input referred third-order intercept	IIP3	Minimum Gain (Maximum AGC)		5	7	dBm
Input referred second-order intercept	IIP2	Minimum Gain (Maximum AGC)	41	47	55	dBm
Gain flatness over frequency	GF	Input freq=250 to 2320MHz		8	10	dB
IQ amplitude balance	IQAB			0.2	0.5	dB
IQ phase balance	IQPB			0.3	0.5	Deg
Minimum voltage conversion gain	Gv(min)	AGC set to maximum (3.3 V)		4		dB
Maximum voltage conversion gain	Gv(max)	AGC set to minimum (0.1V)		82		dB
Voltage conversion gain step	Gv(step)			0.2		dB
Matched input resistance	R_{IN}	After matching		75		Ω
Power up setting time	PUST			1		ms
Input reflection coefficient	S11	After matching		-8	-7	dB

Table 7-5. **Frequency Synthesizer Characteristics** (VDD = 3 to 3.6 V, TA = -25 to 85 °C, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SW}	RX Switch on time			200		us
f_{RFLO}	synthesizer frequency		250		2320	MHz
PN1	Phase noise	Δf=1kHz		-85	-75	dBc/Hz
PN2		Δf=10kHz	-100	-95	-90	dBc/Hz
PN3		Δf=100kHz	-110	-105	-100	dBc/Hz
PN4		Δf=1MHz	-138	-133	-130	dBc/Hz

Table 7-6. Baseband LPF and Output Amplifier Characteristics

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3 dB baseband filter bandwidth	BBF(3dB)		4		40	MHz
Cutoff frequency accuracy at -3dB	FC				+/-5	%
LPF 2fc attenuation	LPF ATT1		25			dB
Flatness	FLTN			0.5	1	dBpp
Group delay	Td(g)			2		ps
Parameter	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Maximum differential output voltage		Clipping level		0.9*VDD		Vpp
Output common mode voltage			0.3*VDD	0.5*VDD	0.6*VDD	V
Differential Output offset voltage				30		mV
IQ output impedance			25	45	55	Ω
Output Amplifier minimum load impedance			1K			Ω
Output Amplifier maximum Load capacitance					10	pF

Table 7-7. XTAL Characteristics

(VDD = 3 to 3.6 V, TA = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
XTAL differential output voltage			680		mVpp
XTAL common mode voltage			0.55		V

8. Control Interface

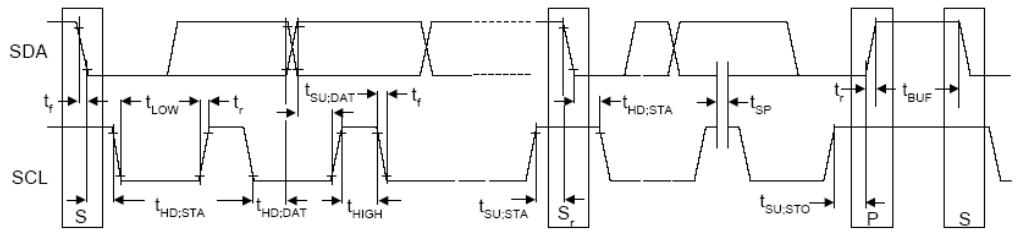
Table 8-1. I2C Address Selection

MA1	MA0	ADD input voltage
0	0	0 V ~0.1VDD
0	1	Open
1	0	0.4VDD~0.6VDD
1	1	0.9VDD~VDD

Table 8-2. I2C bus Characteristics

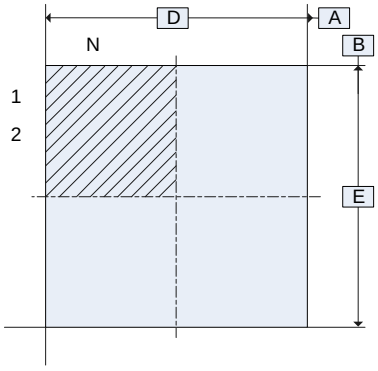
(VDD = 3 to 3.6 V, TA = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	Test Condition	MIN	TYP	MAX	UNIT
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			µs
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$t_{HD, STA}$		0.6			µs
LOW Period of SCL Clock	t_{LOW}		1.3			µs
HIGH Period of SCL Clock	t_{HIGH}		0.6			µs
PARAMETER	**SYMBOL**	**Test Condition**	**MIN**	**TYP**	**MAX**	**UNIT**
Data Setup Time	$t_{SU,DAT}$		100			ns
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
SCL and SDA Rise and Fall Time	t_f,t_f				300	ns
Setup Time for a Repeated START Condition	$t_{SY,STA}$		0.6			µs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Capacitive Load for each Bus Line	C_B				400	pF

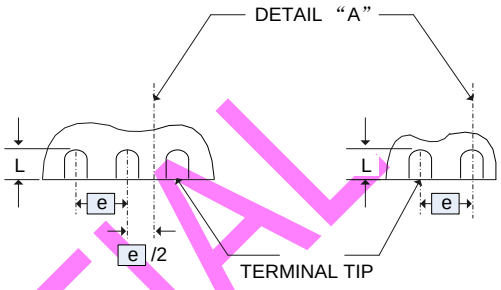


I2C Timing Diagram

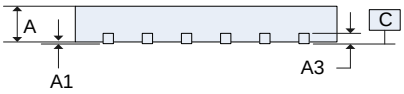
9. Package Outline



TOP VIEW

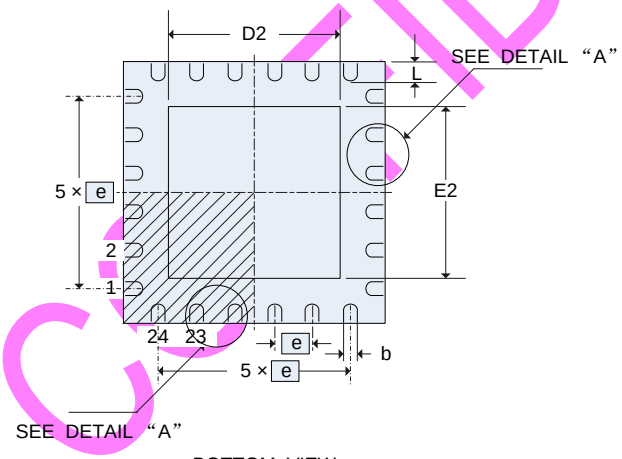


EVEN TERMINAL/SIDE ODD TERMINAL/SIDE



SIDE VIEW

DETAIL "A"

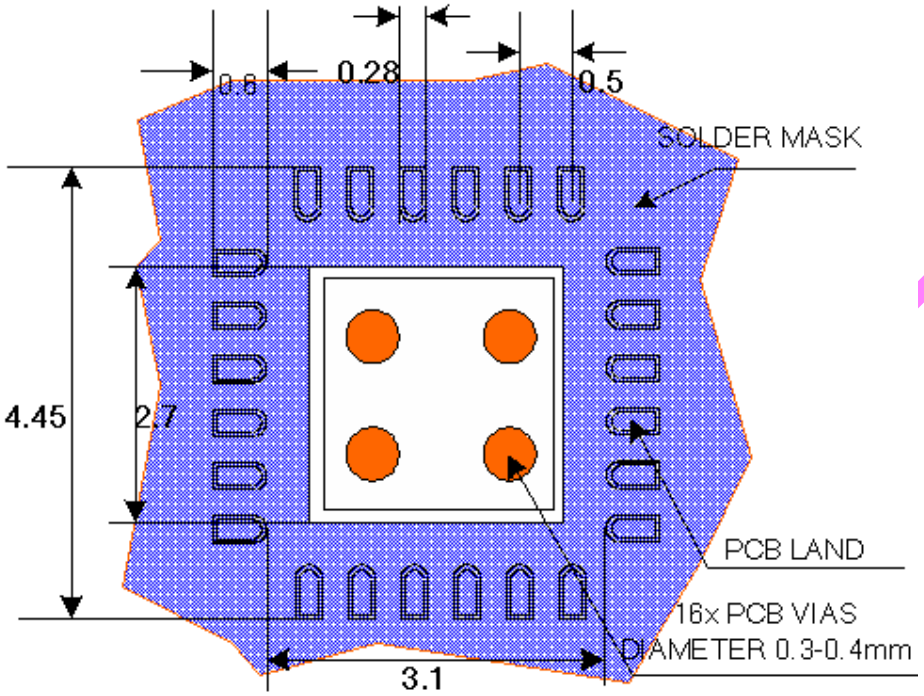


BOTTOM VIEW

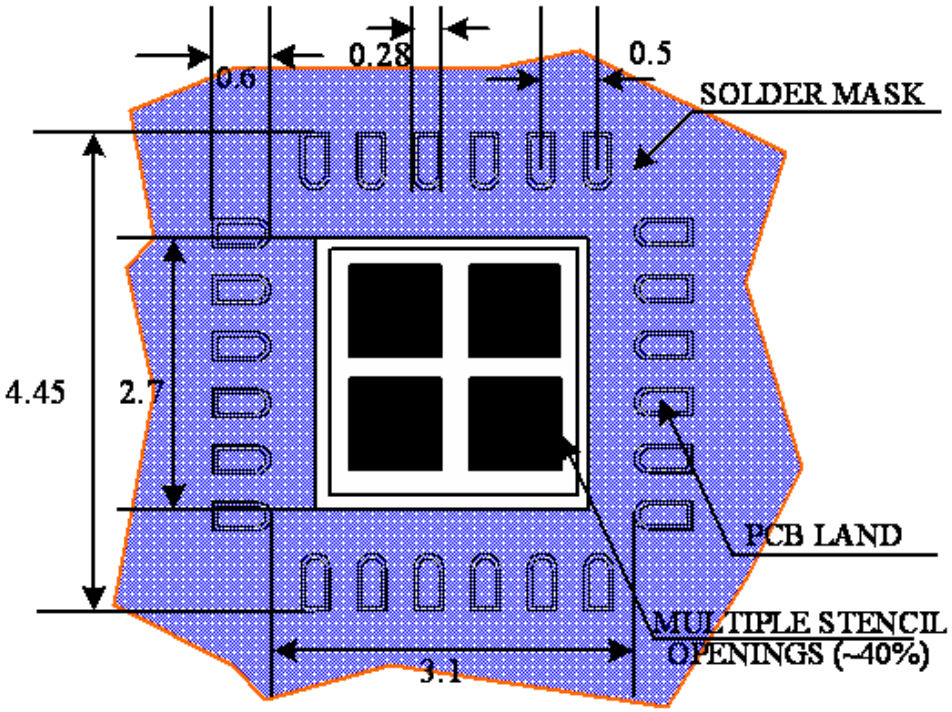
	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.00	2.15	2.25
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

24-Pin 4x4 Quad Flat No-Lead (QFN)

10. PCB land pattern

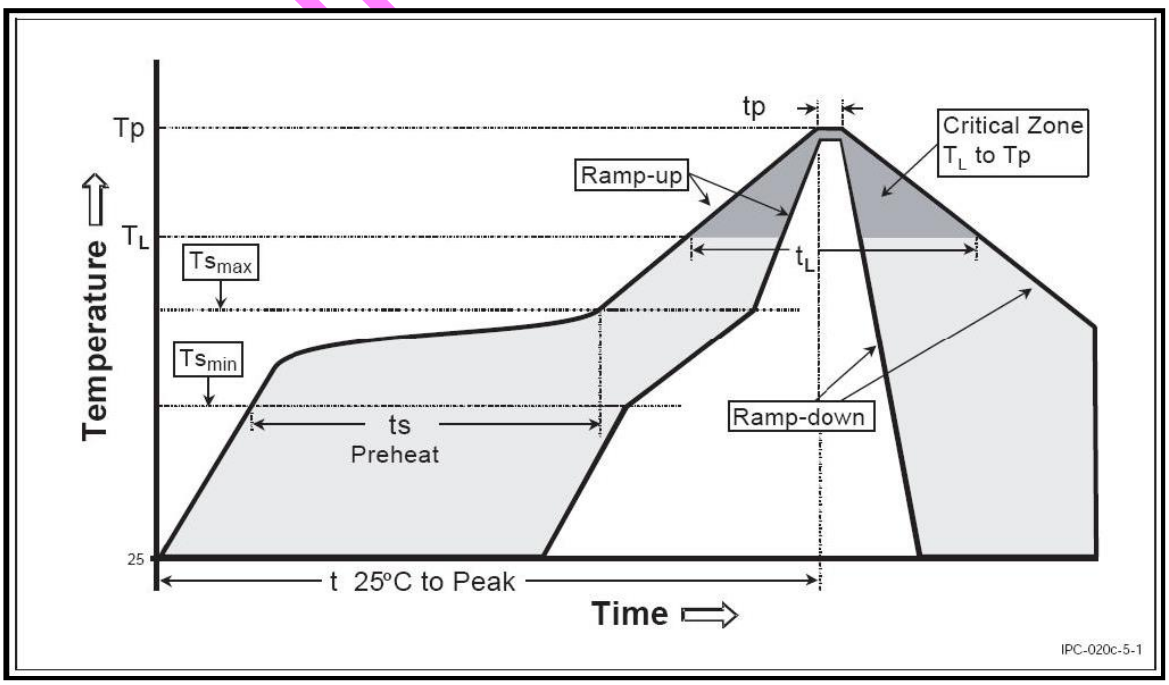


PCB Land Pattern for 24-Pin QFN



PCB Solder Paste Stencil Openings

11. Recommended Reflow Profile



Classification Reflow Profile

Table 11-1. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 10	See Table 11
Time within 5℃ of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25℃ to Peak Temperature	6 minutes max.	8 minutes max.

Table 11-2. Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 11-3. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperatures refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time it will not exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 8-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may still exist.

Note 5: Components intended for use in a "lead-free" assembly process shall be evaluated using the "lead free" classification temperatures and profiles defined in Table8-1~3 whether or not lead free.

Table 11-4. Junction Temperature specification

(VDD =3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
ΘjA	Junction to Ambient Thermal Resistance			29.4		°C/W
T_j	Junction Temperature	Ta (Ambient Temperature) -25 °C	-10	-8.5	-7	°C
T_j	Junction Temperature	Ta (Ambient Temperature) 25 °C	40	41.5	43	°C
T_j	Junction Temperature	Ta (Ambient Temperature) 85 °C	100	101.5	103	°C

Note:

Tj = Ta +ΘjA * Power Consumption, MIN value comes from 3.0v VDD, TYP value comes from 3.3v VDD, MAX value comes from 3.6v VDD.

Table 11-5. Absolute Maximum ratings

Symbol	Description	MIN	MAX	UNIT
VDD	Power supply voltage	-0.3	3.6	V
T_{oper}	Operating ambient Temperature	-25	85	°C
T_j	Junction Temperature		125	°C

12. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and is therefore considered RoHS compliant.

13. ESD Precautions

ESD protection circuitry is contained in this device, but special handling precautions are required.

14. Disclaimer

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