DATA SHEET

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RDA16112

Fully Integrated, Direct Down-Conversion Satellite Receiver for DVB-S,DVB-S2&ABS

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Update History

Rev	Date	Author	History Description
1.0	2013-11-10		The primary datasheet
1.1	2014-03-03		Administrative update

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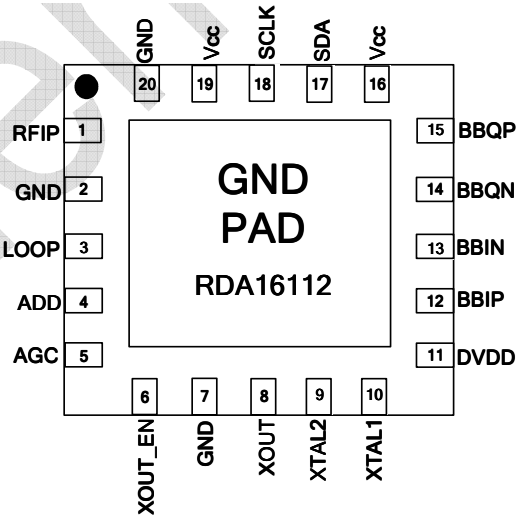
Features

- Single-chip RF-to-baseband Satellite receiver
- CMOS Fully integrated RF front end
- Low noise and wide dynamic range zero-IF receiver
- Input frequency range: 900 to 2200 MHz
- Input signal level: -100 to 5 dBm
- More than 85dB gain control range
- Fully integrated PLL (dividers, charge pump, phase & frequency detectors, loop filters, etc.)
- Integrated RX VCO
- Integrated baseband LPF with selectable cut-off frequency from 4MHz to 40MHz with 1MHz step
- Integrated LNA with RF AGC
- Integrated reference oscillator (27MHz is defult)
- I^2C bus interface
- Automatic gain control
- 0.11μm RF CMOS technology
- 3V to 3.6V operation
- power consumption of less than 500mW
- Lower profile packages:

RDA16112 3×3 mm QFN20

Pin assignment (20pin QFN 3×3 mm)



Applications

- Set-top boxes
- Digital video recorders
- Digital television
- Satellite PC-TV
- SMATV trans-modulators (Satellite Master Antenna TV)

General Description

The RDA16112 is a fully integrated direct conversion RF front end for DVB-S,DVB-S2&ABS digital satellite Reception standard CMOS process. The receiving frequency range is from 900MHz to 2200MHz, and the baseband filter's bandwidth can be selected from 4MHz to 40MHz with 1MHz step.

The RDA16112 consists of a variable gain LNA, quadrature downconverter, variable IF gain amplifiers, variable low-pass filters, reference oscillator, VCOs, synthesizer and output baseband amplifier to drive external ADC.

Based on RDA's some innovative technique, the RDA16112 offers excellent phase noise and very low implementation loss, required for advanced modulation systems such as 8PSK and DVB-S2. This tuner RF IC does not require a balun and its fully integrated design saves valuable board space and simplifies RF layout.

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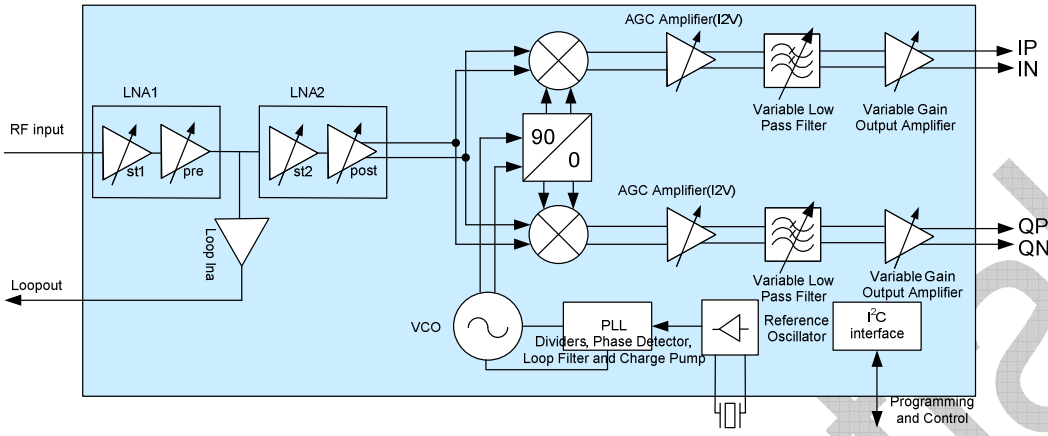
Functional Block Diagram



Functional Description

The loop lna is used to generate the loopout signal. LNA1&LNA2 are on chip variable gain LNAs are used to provide wide tuner dynamic range. A direct conversion architecture is used to convert the RF signal to in-phase and quadrature baseband signals. The signals required for direct conversion are all generated within the chip by a fully integrated PLL and a quadrature LO generator. The frequency of the VCO is set by internal PLL circuits, which are programmable via a 2-wire (I^2C) serial bus. The LO signals are mixed with the RF signal input and then filtered by low-pass filters to remove the upper image produced by the mixer. A variable gain amplifier is then used to adjust the baseband signal levels before processing by the channel selection filters to optimize noise performance and prevent distortion within the filters. The channel select filters are digitally programmable low pass filters with 1MHz step from 4MHz to 40MHz. The output amplifier buffered the signal from the filters to increase the driving capability to the next baseband ADC.

Some innovative technique is used to correct and alleviate DC offsets inherent in direct conversion mixers, the channel select filters and output buffers.

Loop LNA

The loopout lna is used to generate the loopout signal.

LNA1&LNA2

LNA1 is the first lna and receives a signal from the LNB through external matching circuit, the input resistance is matched to 75Ω coaxial cable. The LNA2 is the second lna and is used to provide wide dynamic range, the better noise figure. The gain both of lna1 and lna2 can be programmed with the 2-wire (I^2C) interface to insure wide dynamic range of the receiver.

AGC Amplifier

The AGC Amplifier receives the IQ signals from the quadrature mixer then amplifies them and sends to the base band low pass filter. The gain is also programmed and controlled by the 2-wire (I^2C) interface.

Baseband LPF

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The bansband low-pass filter is designed to have variable cut-off frequency. The bandwidth of the LPF is selectable from 4MHz to 40MHz with 1MHz step. The DC-offset calibration can be carried out controlled by the interface. A innovative technique ensure the filter's bandwidth variety within 5%.

Reference Oscillator

The oscillator is on-chip integrated and both the crystal and crystal oscillator are supported. The 27MHz is recommended. The centre oscillation frequency can be adjusted accurately with the XAFC pin (optional function).

VCO

The receiver integrates two VCOs which ensure covering the full receiving frequency from 900MHz to 2200MHz. The two VCOs can be switched between each other with relevant register and the VCO's band is programmed using 2-wire (I^2C) interface. The first VCO oscillates from 3560MHz to 6380MHz, the second oscillates from 5940MHz to 9250MHz. After divided by four, eight or sixteen, lo signal from 250(4000/16)MHz to 2150(8600/4)can be obtained.

LO frequency	Used VCO	Divider	Note
950(3800/4)≤F≤1538(6152/4)	VCO1	4	**VCO1** oscillates from 3560MHz to 6380MHz.
1539(6156/4)≤F≤2150(8600/4)	VCO2	4	**VCO2** oscillates from 5940MHz to 9250MHz

PLL

The fractional-N frequency synthesizer use 27MHz reference as default. The dividers, loop filters, phase&frequency detector, charge pump are all integrated on chip.

Baseband Output Amplifier

Class-AB architecture is selected for the output buffer, this makes it more flexible to the next Baseband solution's input load. The gain of this stage can also be programmed with interface to farther increase the receiver dynamic.

I^2C interface

The interface is the control unit of all the analog blocks, it is provided for configuration and monitoring all internal registers, the I^2C bus consists of two wires: serial clock line (SCL) and serial data line (SDA). The LNA's gain, AGC, baseband LPF's bandwidth, VCO's and crystal oscillator's current, VCO's oscillation frequency are all controlled by the 2-wire interface.

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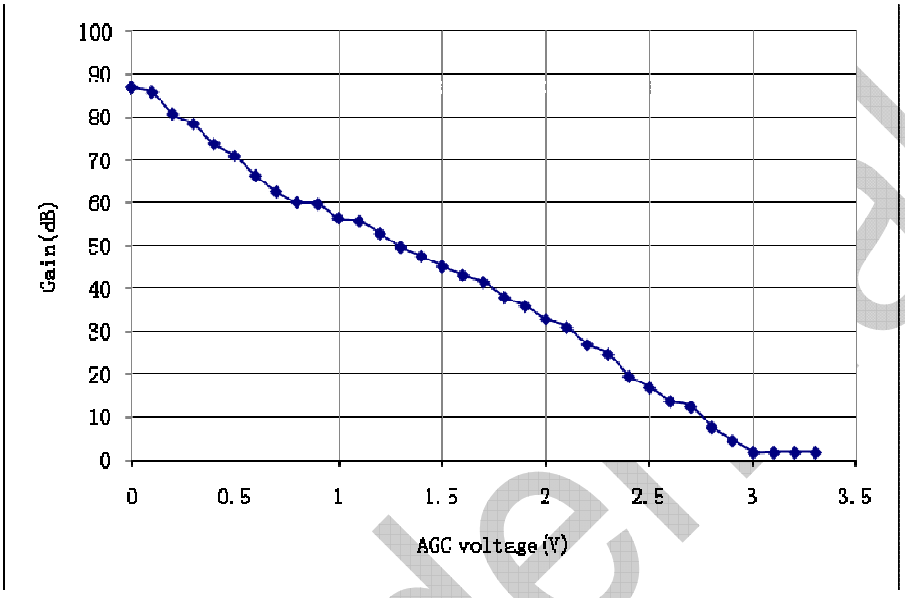
Direct AGC control

Through the AGC pin input, the receiver chain's gain can be directly controlled by the baseband solutions. The receiver gain changed inversely with the AGC control signal, this means that when AGC signal goes high, the receiver gain will drop to relevant level and vice versa.



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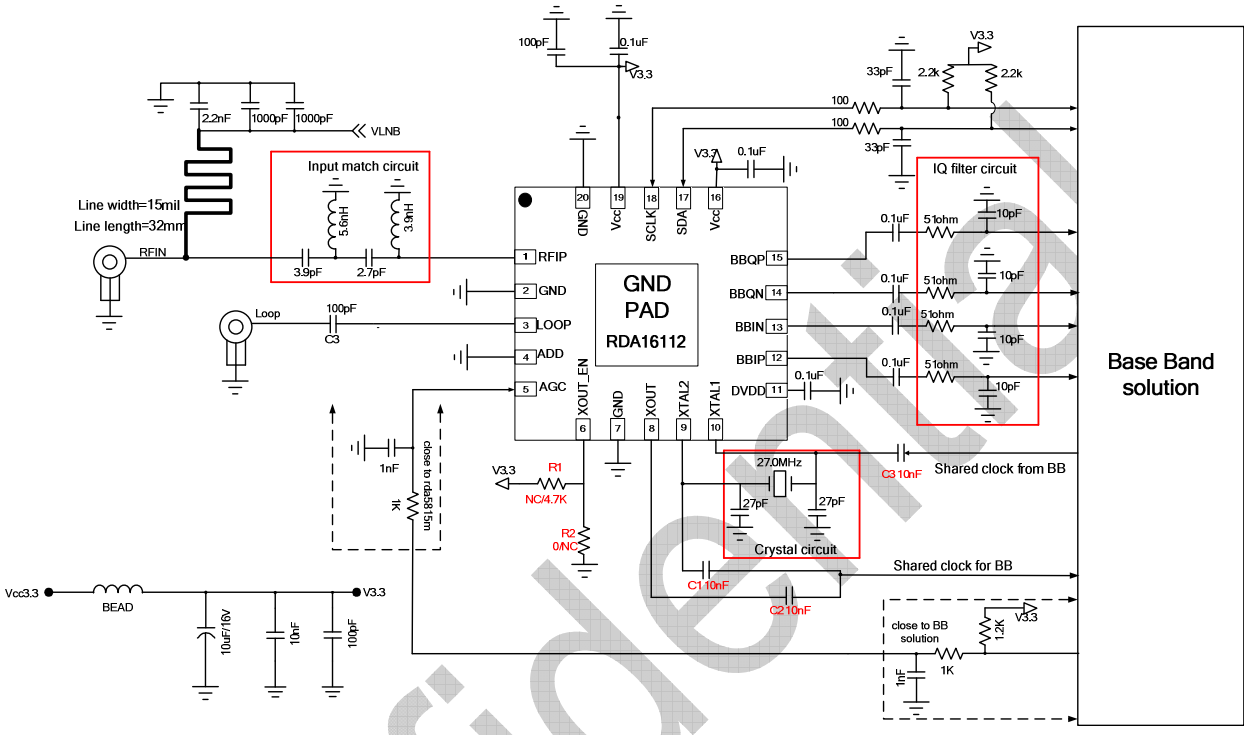
Typical application circuit

Application circuit



Note:

1、The input match circuit

This circuit is optional. If it is used or not, according to the performance requirement .

There will have better S11 and reduce the low frequency block with input match circuit.

2、IQ filter circuit

This circuit is optional. If this circuit is to be use or not according to the test result of different demodulator chip and pcb.

3、Crystal circuit

The value of load capacitance is determined by the crystal parameter.

4、Clock share

Function		ON	OFF
Use BB's clock		Connected to XTAL1 C3=10nF	Delete C3
Share clock for BB (Use xout and xtal2 are both ok)	Xout	R1=4.7K and connected to Vcc, Delete R2 C2=10nF Delete C1	Delete R1,R2,C1,C2
	XTAL2	R2=0 and connected to GND, Delete R1 C1=10nF Delete C2	

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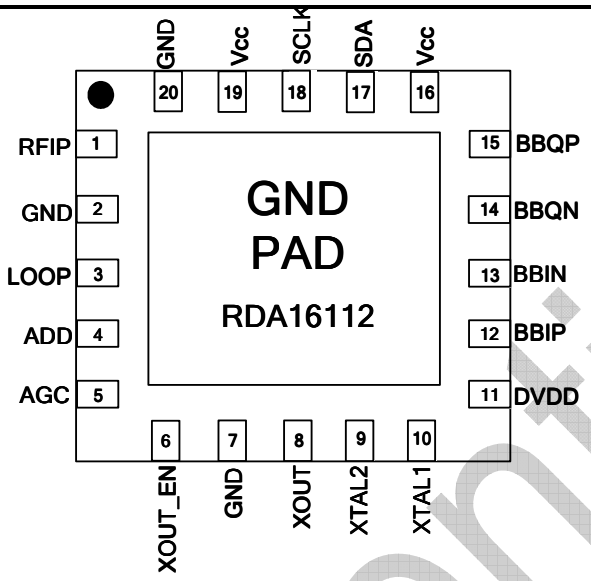
If these circuits are used or not, according to the solution requirement and test result.

Pin Description



Pin number	Name	I/O	DESCRIPTION
1	RFIP	I	RF Positive Input
2	GND.		
3	LOOP.	O	LOOPOUT
4	ADD	I	I2C bus address selection terminal. Allowing the use of more than one device per I2C bus system by the voltage on this pin. See Table 8 for programming details.
5	AGC	I	AGC control input from baseband solutions
6	XOUT_EN	I	To control the XOUT pin to send out the buffed xtal signal or not If GND,XOUT=Off; If VDD,XOUT=On
7	GND.		
8	XOUT	I	Buffered Crystal oscillator output for BaseBand solution
9	XTAL2	I/O	Connect to Crystal (27MHz is recommanded)
10	XTAL1	I/O	Connect to Crystal (if using external crystal oscillator, this pin connect to the oscillator's output)
11	DVDD	O	Output of the supply voltage for Digital, Connected to cap
12	BBIP	O	Positive Baseband I Channel Out
13	BBIN	O	Negative Baseband I Channel Out
14	BBQN	O	Negative Baseband Q Channel Out
15	BBQP	O	Positive Baseband Q Channel Out
16	Vcc	I	Supply voltage for 16112. Connected to 3.3 V.

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17	SDA	I/O	Serial data input/output, connected to 3.3V with 10kΩ resistor
18	SCLK	I	Serial clock input
19	Vcc	I	Supply voltage for 16112. Connected to 3.3 V.
20	GND.		

Electrical Specifications

Table 1 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	AVDD	3	3.3	+3.6	V
Ambient Temperature	T_A	-25	27	+85	℃

Table 2 DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V_{IL}	0		0.3*VDD	V
CMOS High Level Input Voltage	V_{IH}	0.7*VDD		VDD	V
CMOS Threshold Voltage	V_{TH}		0.5*VDD		V

Table 3 Power consumption specification

(VDD =3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
ICC	Receiver on			150	155	mA
ICC(standby)	tuner Disabled	PDN=1,Enable=0,Rxon=0		29		mA

Table 4 System Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	f_{IN}		900		2200	MHz
Minimum RF input	RFIL	4.42MS/s, QPSK3/4,noise free		-99	-96	dBm
Maximum RF input	RFIH	4.42MS/s, QPSK3/4, noise free		5	7	dBm
Minimum RF input	RFIL	45MS/s, QPSK3/4, noise free		-87	-85	dBm
Maximum RF input	RFIH	45MS/s, QPSK3/4, noise free		5	7	dBm
IQ amplitude balance	IQAB			0.2	0.5	dB
IQ phase balance	IQPB			0.3	0.5	Deg
Minimum voltage conversion gain	Gv(min)	AGCIN set to maximum (3.3 V)		5		dB
Maximum voltage	Gv(max)	AGCIN set to minimum		85		dB

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conversion gain		(0.1V)				
Voltage conversion gain step	Gv(step)			0.2		dB
Matched input resistance	R_{IN}	After matching		75		Ω
Power up setting time	PUST			5		ms
Input reflection coefficient	S11	After matching		-8	-7	dB

Parameter		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Main Channel	Noise Figure	NF	Max Gain (Minimum AGC)		3.2	4.8	dB
	Input refered third-order intercept	IIP3	Minimum Gain (Maximum AGC)		7	9	dBm
	Input refered econd-order intercept	IIP2	Minimum Gain (Maximum AGC)		72	74	dBm
	Gain flatness over frequency	GF	Input freq 900 to 2250MHz		4	5	dB

Parameter		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Loop Channel	Noise Figure	NF	Max Gain (Minimum AGC)	5.5	5.7	7.5	dB
	Input refered third-order intercept	IIP3	Minimum Gain (Maximum AGC)	2	4	6	dBm
	Input refered second-order intercept	IIP2	Minimum Gain (Maximum AGC)		57		dBm
	Gain	Gain	Input freq 900 to 2250MHz	2	3	3.5	dB

Table 5 Frequency Synthesizer Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SW}	RX Switch on time			200		us
f_{RFLO}	synthesizer frequency		900		2200	MHz
PN1	Phase noise	Δf=1kHz		-88	-81	dBc/Hz
PN2		Δf=10kHz	-100	-95	-90	dBc/Hz
PN3		Δf=100kHz	-110	-105	-100	dBc/Hz
PN4		Δf=1MHz	-138	-133	-130	dBc/Hz

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Table 6 Baseband LPF and Output Amplifier Characteristics

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3 dB baseband filter bandwidth	BBF(3dB)		4		40	MHz
Cutoff frequency accuracy at -3dB	FC				+/-5	%
LPF 2fc attenuation	LPF ATT1		25			dB
Flatness	FLTN			0.5	1	dBpp
Group delay	Td(g)			2		ps
Maximum differential output voltage		Clipping level		0.9*VDD		Vpp
Output common mode voltage			0.3*VDD	0.5*VDD	0.6*VDD	V
Differential Output offset voltage				30		mV
IQ output impedance			25	45	55	Ω
Output Amplifier minimum load impedance			1K			Ω
Output Anplifier maximum Load capacitance					10	pF

Table7 XTAL&XOUT Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
XTAL differential output voltage		550	1200	1420	mVpp
XTAL common mode voltage			0.6		V

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
XOUT differential output voltage			1250		mVpp
XOUT common mode voltage			0.8		V

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Control Interface

Table 8 I²C Address selection

MA1	MA0	ADD input voltage
0	0	0 V
1	0	Open
1	1	VDD

Table 9 I²C bus characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

PARAMETER	SYMBOL	Test Condition	MIN	TYP	MAX	UNIT
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			μs
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$T_{HD, STA}$		0.6			μs
LOW Period of SCL Clock	t_{LOW}		1.3			μs
HIGH Period of SCL Clock	t_{HIGH}		0.6			μs
Data Setup Time	$t_{SU,DAT}$		100			ns
Data Hold Time	$t_{HD,DAT}$		0		0.9	μs
SCL and SDA Rise and Fall Time	t_r,t_f				300	ns
Setup Time for a Repeated START Condition	$t_{SY,STA}$		0.6			μs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs
Capacitive Load for each Bus Line	C_B				400	pF

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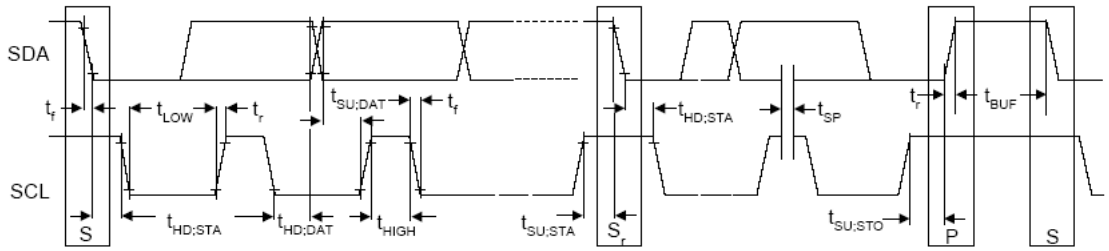

I^2C Timing Diagram

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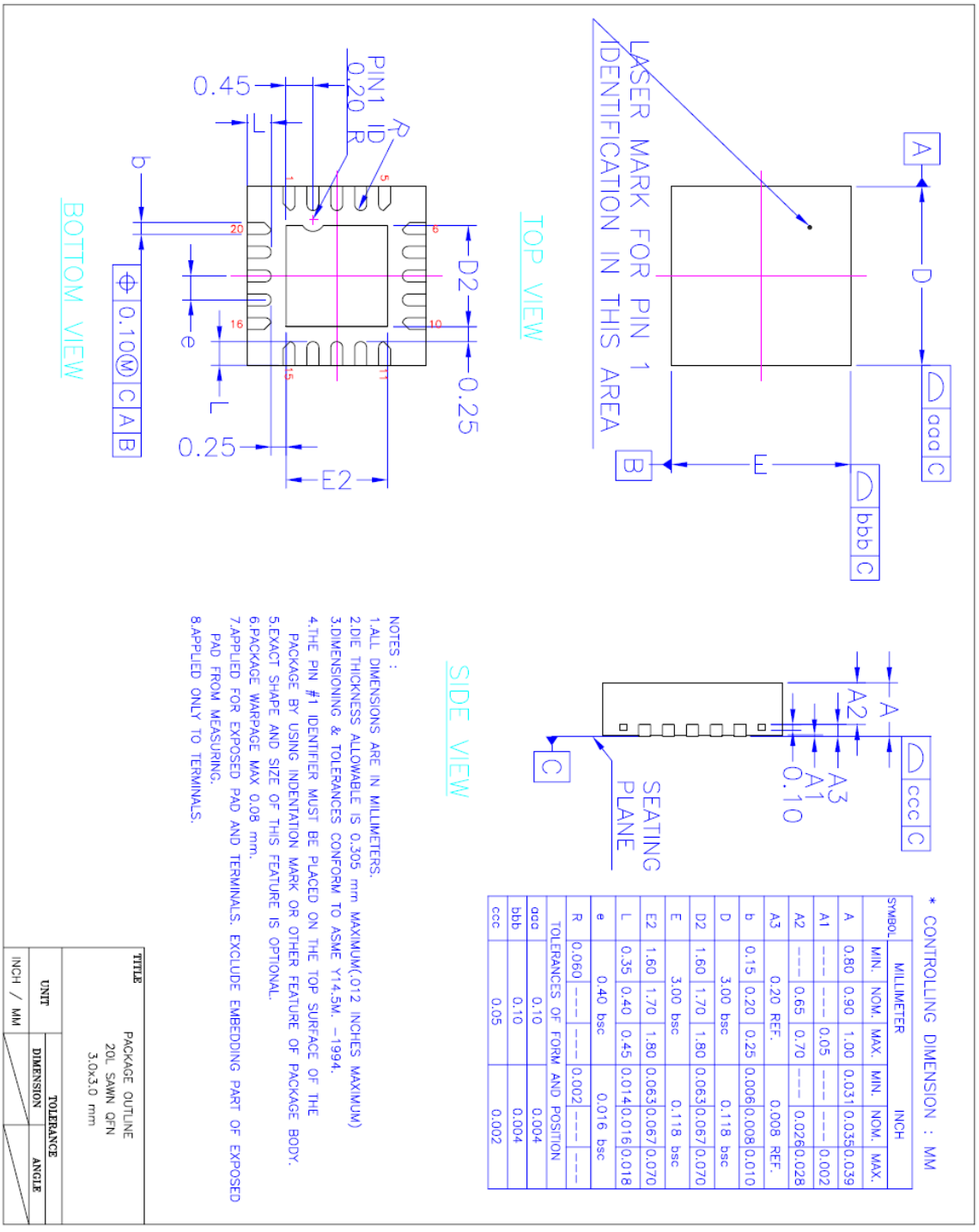
Package Outline



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	----	----	0.05	----	----	0.002
A2	----	0.65	0.70	----	0.026	0.028
A3		0.20 REF.			0.008 REF.	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		3.00 bsc			0.118 bsc	
D2	1.60	1.70	1.80	0.063	0.067	0.070
E		3.00 bsc			0.118 bsc	
E2	1.60	1.70	1.80	0.063	0.067	0.070
L	0.35	0.40	0.45	0.014	0.016	0.018
e		0.40 bsc			0.016 bsc	
R	0.060	----	----	0.002	----	----
TOLERANCES OF FORM AND POSITION						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

20-Pin 3x3 Quad Flat No-Lead (QFN)

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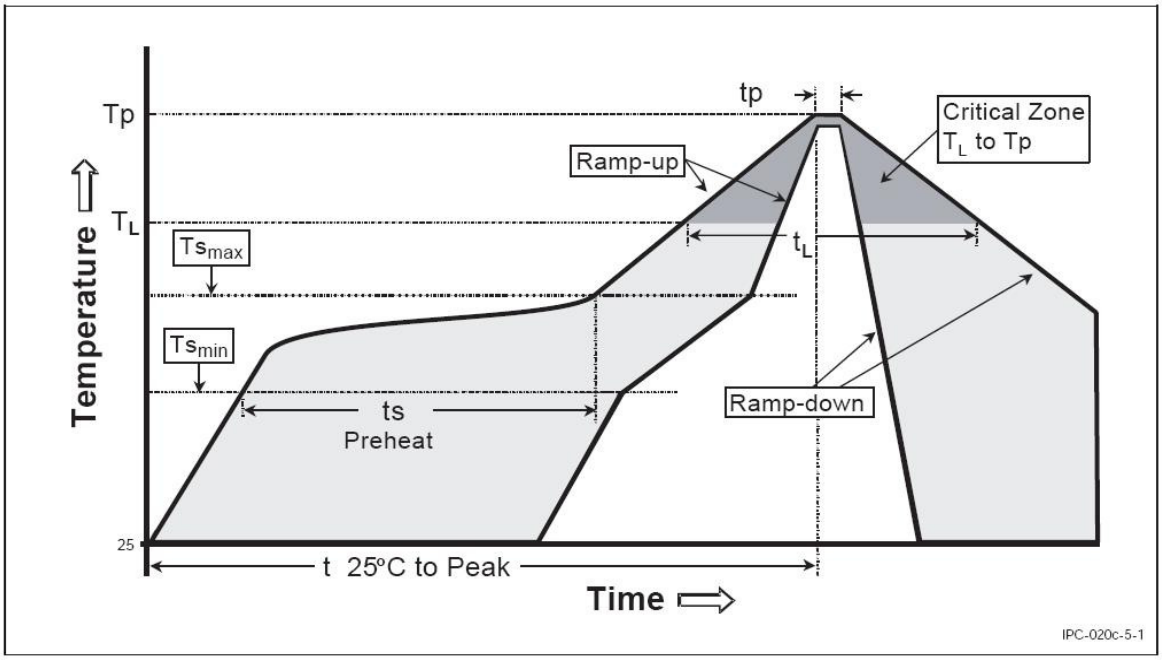
Solder Mounting Condition



Classification Reflow Profile

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Table-I Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

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Table – III Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" classification temperatures and profiles defined in Table-I II III whether or not lead free.

Table 10 Junction Temperature specification

(VDD =3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
ΘjA	Junction to Ambient Thermal Resistance			29.4		℃/W
T_j	Junction Temperature	Ta (Ambient Temperature) -25 ℃	-10	-8.5	-7	℃
T_j	Junction Temperature	Ta (Ambient Temperature) 25 ℃	40	41.5	43	℃
T_j	Junction Temperature	Ta (Ambient Temperature) 85 ℃	100	101.5	103	℃

Note: Tj = Ta +ΘjA * Power Consumption, MIN value comes from 3.0v VDD, TYP value comes from 3.3v VDD, MAX value comes from 3.6v VDD.

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Table 11 Absolute Maximum ratings

Symbol	Description	MIN	MAX	UNIT
VDD	Power supply voltage	-0.3	3.6	V
T_{oper}	Operating ambient Temperature	-25	85	℃
T_j	Junction Temperature		125	℃

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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