

DATA SHEET

RDA5816sw

**Fully Integrated Satellite Dual Receiver
for DVB-S2 with RF switch integrated**

Update History

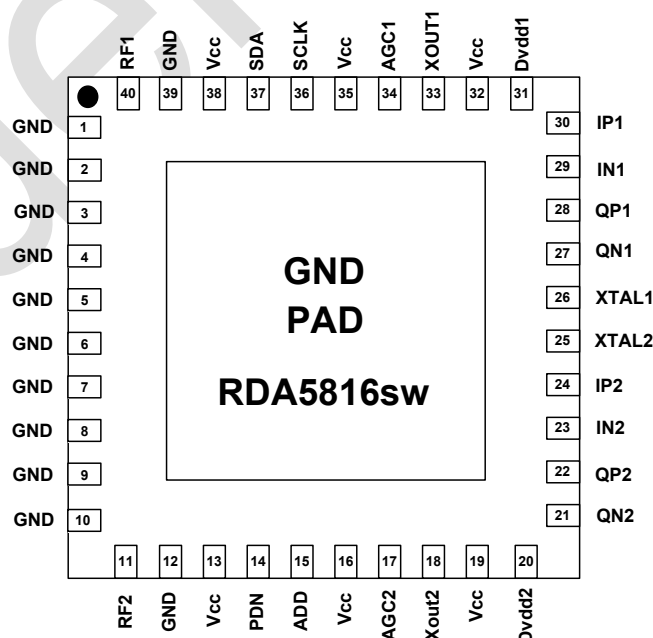
Rev	Date	Author	History Description
1.0	2013-05-15		The primary datasheet
1.1	2013-05-31		Add the internal block diagram
1.2	2013-06-25		Add the description of RF switches control
1.2	2024-10-15		Higher spec limit for Large signal handling/IP2 & 3 and phase noise

Features

- Single-chip Two channels RF-to-baseband Satellite receiver
- RF switches integrated
- CMOS Fully integrated RF front end
- Low noise and wide dynamic range zero-IF receiver
- Input frequency range: 900 to 2200 MHz
- Input signal level: -80 to 0 dBm
- More than 80dB gain control range
- Fully integrated PLL (dividers, charge pump, phase & frequency detectors, loop filters, etc.)
- Integrated RX VCO
- Integrated baseband LPF with selectable cut-off frequency from 4MHz to 40MHz with 1MHz step
- Integrated LNA with RF AGC
- Integrated reference oscillator (27MHz as default)
- I²C bus interface
- Automatic gain control
- 0.11μm RF CMOS technology
- 3V to 3.6V operation
- 5×5 mm QFN40

Applications

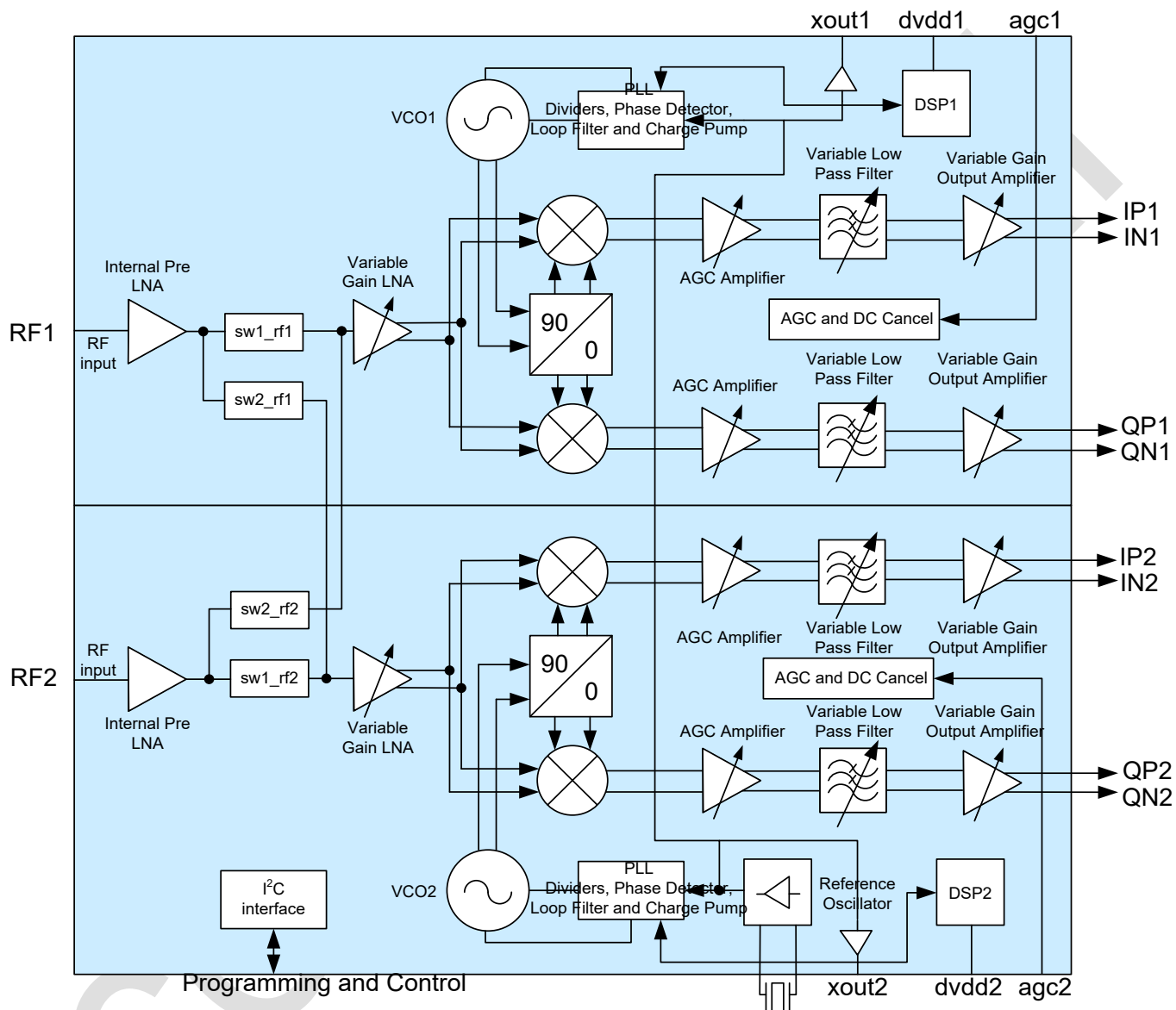
- Digital video recorders
- Digital television
- Satellite PC-TV
- Set-top boxes



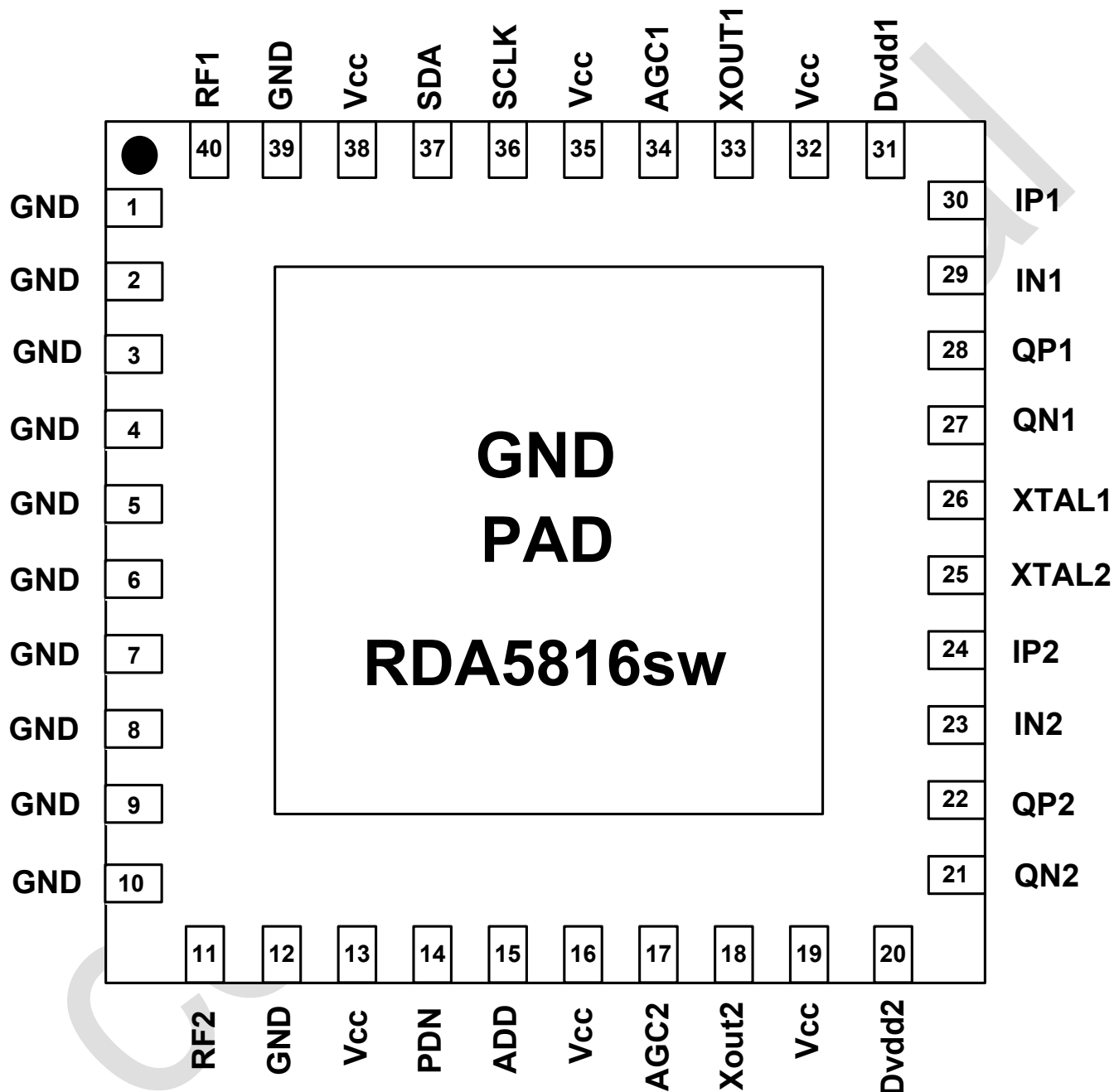
General Description

The RDA5816sw is a RF switches integrated two-channel fully integrated direct-conversion RF front end for DVB-S2 application. There have two channels integrated in rda5816sw with each channel separately controlled through the I2C bus. With the RF switches, the two RF input signals can be switched between each other after setting the different switching modes. The receiving frequency range is from 900MHz to 2200MHz, and the baseband filter bandwidth can be selected from 4MHz to 40MHz with 1MHz step.

Functional Block Diagram



Pin Description



Pin number	Name	I/O	DESCRIPTION
1~10,12,39	GND		Connected to Ground
11	RF2	I	The RF input pin for the channel 2
13	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
14	PDN	I	Chip power control If low, Receiver totally power down, including the crystal oscillator. If High, the chip is enabled.
15	ADD	I	I2C bus address selection terminal. Allowing the use of more than one device per I2C bus system by the voltage on this pin. See Table 8 for programming details.
16	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
17	AGC2	I	AGC control input for the channel 2
18	Xout2	O	Buffered Crystal oscillator output for demod2
19	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
20	Dvcc2	O	Output of the supply voltage for channel2's dsp, Connected to cap
21	QN2	O	Negative Base-Band Q Channel2 Out
22	QP2	O	Positive Base-Band Q Channel2 Out
23	IP2	O	Positive Base-Band I Channel2 Out
24	IN2	O	Negative Base-Band I Channel2 Out
25	Xtal2	I/O	Connect to Crystal (27MHz is recommended)
26	Xtal1	I/O	Connect to Crystal (27MHz is recommended)
27	QN1	O	Negative Base-Band Q Channel1 Out
28	QP1	O	Positive Base-Band Q Channel1 Out
29	IN1	O	Positive Base-Band I Channel1 Out
30	IP1	O	Negative Base-Band I Channel Out
31	Dvcc1	O	Output of the supply voltage for channel1's DSP, Connected to cap
32	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
33	Xout1	O	Buffered Crystal oscillator output for demod1
34	AGC1	I	AGC control input for the channel 1
35	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
36	SCLK	I	Serial clock input
37	SDA	I/O	Serial data input/output, connected to 3.3V with 10kΩ resistor
38	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
40	RF1	I	The RF input pin for the channel 2

Electrical Specifications

Table 1 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	AVCC	3	3.3	+3.6	V
Ambient Temperature	T _A	-25	27	+85	°C
Junction Temperature	T _J		125		°C

Table 2 DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V _{IL}	0		0.3*VCC	V
CMOS High Level Input Voltage	V _{IH}	0.7*VCC		VCC	V
CMOS Threshold Voltage	V _{TH}		0.5*VCC		V

Table 3 Power consumption specification (VCC = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Symbol	Description	Condition	TYP	UNIT
ICC	Both Channels ON	Normal work	300	mA
ICC	One Channel ON	Normal work	155	mA
ICC	Sleep mode	PDN = 1, Enable=0	6	mA
ICC	Sleep mode	PDN = 0	250	uA

Table 4 System Characteristics (VCC = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	f _{IN}		900		2200	MHz
Noise Figure	NF	Maximum Gain		3.5	5.5	dB
Input referred third-order intercept	IIP3	Minimum Gain	9.5	10	11	dBm
Input referred second order intercept	IIP2	Minimum Gain		40		dBm
Isolation of RF1 and RF2				60		dB
Gain flatness	GF	900MHz to 2200MHz		4	5	dB
IQ amplitude balance	IQAB				0.5	dB
IQ phase balance	IQPB				0.5	Deg
Minimum voltage conversion gain	Gv(min)	AGCIN set to maximum (3.3 V)		-2		dB
Maximum voltage conversion gain	Gv(max)	AGCIN set to minimum (0.1V)		85		dB
Voltage conversion gain step	Gv(step)			0.2		dB
Matched input resistance	R _{IN}	After matching		75		Ω
Power up setting time	PUST			1		ms
Input reflection coefficient	S11	After matching		-10		dB

Table5 Frequency Synthesizer Characteristics (VCC=3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t _{SW}	RX Switch on time			200		us
f _{RFLO}	synthesizer frequency		900		2200	MHz
PN1	Phase noise	Δf=1kHz		-88	-80	dBc/Hz
PN2		Δf=10kHz	-100	-95	-90	dBc/Hz
PN3		Δf=100kHz	-110	-105	-100	dBc/Hz
PN4		Δf=1MHz	-138	-133	-130	dBc/Hz

Table 6 Baseband LPF and Output Amplifier Characteristics

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3 dB baseband filter bandwidth	BBF(3dB)		4		40	MHz
Cutoff frequency accuracy at -3dB	FC				+/-5	%
LPF 2fc attenuation	LPF ATT1		25			dB
Flatness	FLT _N			0.5	1	dBpp
Group delay	Td(g)			2		ps
Maximum differential output voltage		Clipping level		0.9*VCC		V _{pp}
Output common mode voltage			0.3*VCC	0.5*VCC	0.6*VCC	V
Differential Output offset voltage				30		mV
IQ output impedance			25	45	55	Ω
Output Amplifier minimum load impedance			1K			Ω
Output Amplifier maximum Load capacitance					10	pF

Table 7 Crystal Characteristics (VCC = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
differential output voltage	xtal2		810		mV _{pp}
	xtal1		800		
	xout2		800		
	xout1		727		
common mode voltage	xtal2		0.4		V
	xtal1		0.5		
	xout2		0.81		
	xout1		0.81		

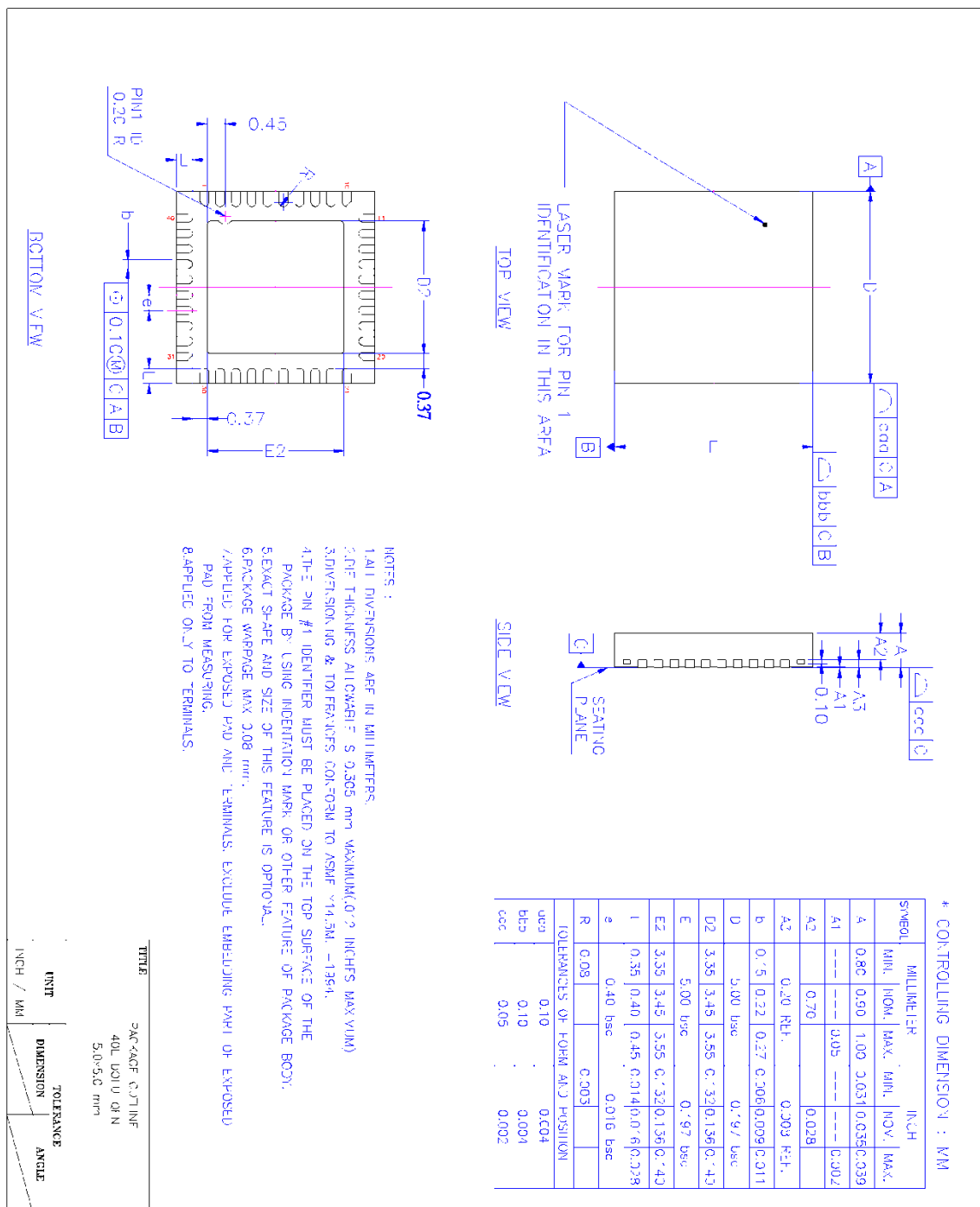
Table 8 I²C Address selection

ADD input voltage	I2C Address				
	bit<7:4>	bit<3>	bit<2>	bit<1>	
	0001	MA1	MA0	0	1
0 V ~ 0.1 VCC	0001	0	0	channel1	channel2
open	0001	0	1	channel1	channel2
0.9 VCC ~ VCC	0001	1	1	channel1	channel2

Table 9 RF Switch control function

sw1_rf1 (65h<2>)	sw2_rf2 (65h<1>)	sw1_rf2 (65h<2>)	sw2_rf2 (65h<1>)	RF switch function
on	off	on	off	RF1 to BB1, RF2 to BB2
on	on	off	off	RF1 to BB1, RF1 to BB2
off	off	on	on	RF2 to BB2, RF2 to BB1

Package Outline



40-Pin 5x5 Quad Flat No-Lead (QFN)

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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