DATA SHEET

RDA16110SW

Fully Integrated Satellite Dual Receiver for DVB-S/S2 with RF switch integrated

Update History

Rev	Date	Author	History Description
1.0	2013-12-12		The primary datasheet
1.2	2014-02-25		Pin definiation correction (pg 10)

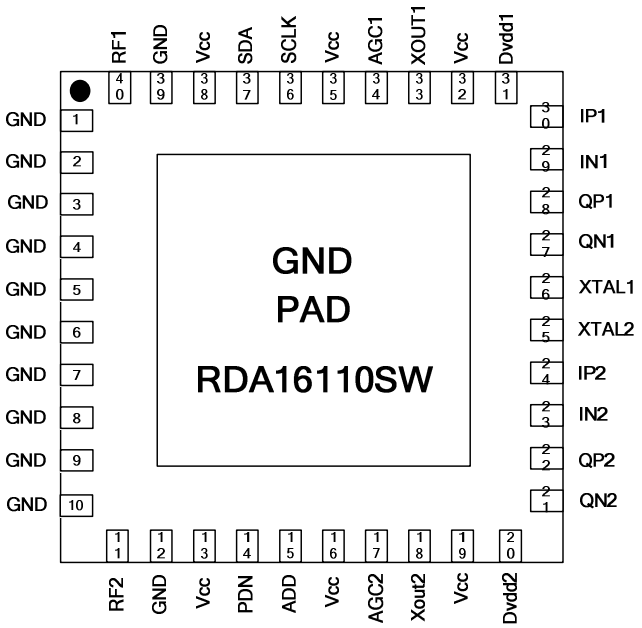
Features

- Single-chip Two channels RF-to-baseband Satellite receiver
- RF switches integrated
- CMOS Fully integrated RF front end
- Low noise and wide dynamic range zero-IF receiver
- Input frequency range: 900 to 2200 MHz
- Input signal level: -80 to 0 dBm
- More than 80dB gain control range
- Fully integrated PLL (dividers, charge pump, phase & frequency detectors, loop filters, etc.)
- Integrated RX VCO
- Integrated baseband LPF with selectable cut-off frequency from 4MHz to 40MHz with 1MHz step
- Integrated LNA with RF AGC
- Integrated reference oscillator (27MHz is defult)
- I^2C bus interface
- Automatic gain control
- 0.11μm RF CMOS technology
- 3V to 3.6V operation
- 5×5 mm QFN40

Applications

- Set-top boxes
- Digital video recorders
- Digital television
- Satellite PC-TV

Pin assignment (40 pin QFN 5×5 mm)



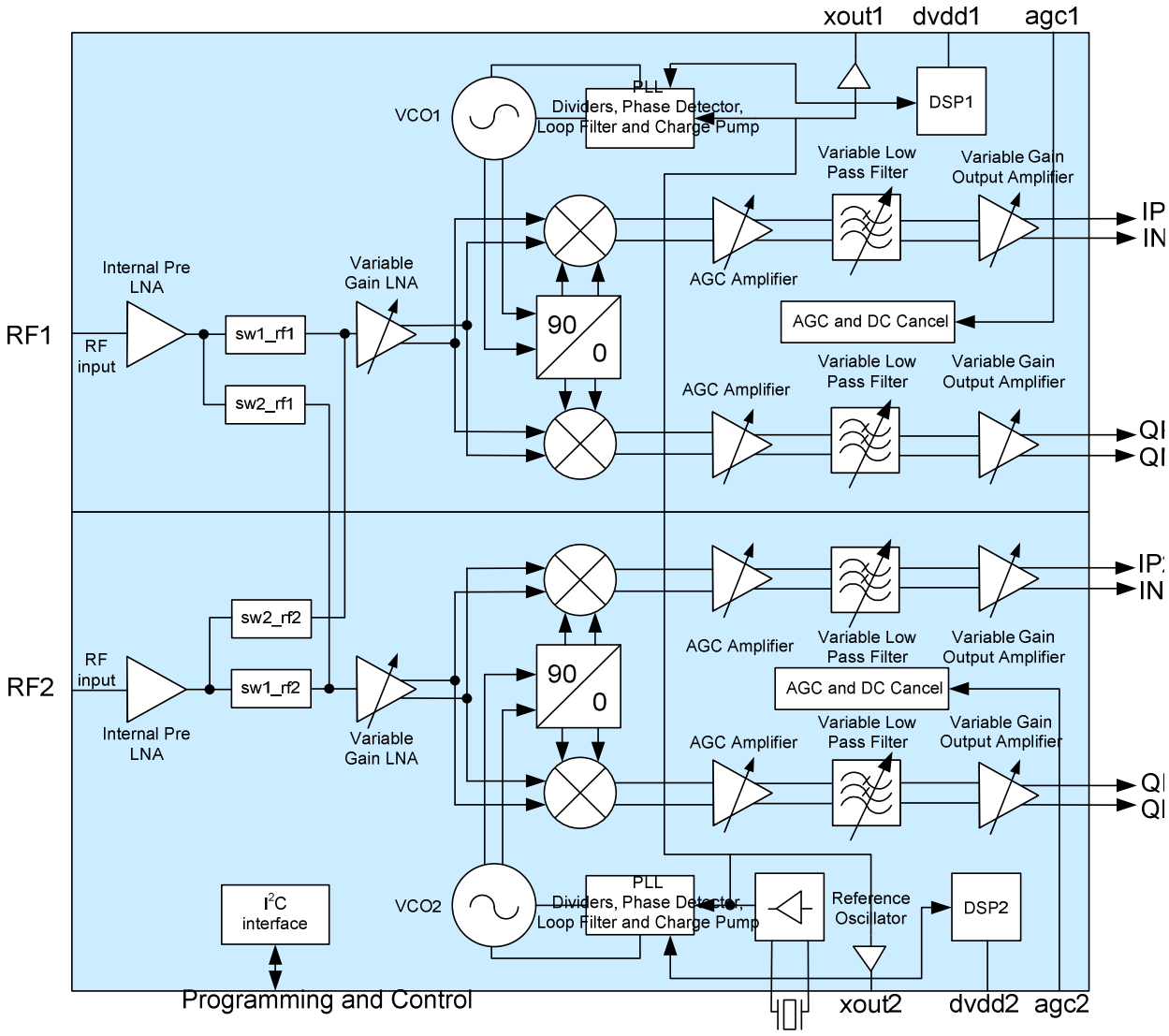
General Description

The RDA16110SW is a two-channels fully integrated direct-convertion RF front end for DVB-S2 application.

There have two channels intergrated in RDA16110SW, each channel can be saperately controlled trough the I2C bus. With the RF switches, the two RF input signals can be switched between each other after setting the different switching modes.

The receiving frequency range is from 900MHz to 2200MHz, and the baseband filter's bandwidth can be selected from 4MHz to 40MHz with 1MHz step.

Functional Block Diagram



Function Descriptions

As a dual-channel tuner product, RDA16110SW is made up of two individual RF cores in the silicon chip, only the Xtal clock and I2C bus are shared by the two channels. There are RF switches build at the front of variable gain LNA which enable receive of dual channel via dual RF inputs or any single RF Input. These RF switches are controlled via IIC bus.

Of each channel, there are two stages of LNA circuit in front of mixer – Internal Pre LNA and Variable Gain LNA. Variable Gain LNA is used to provide wide tuner dynamic range. Direct conversion architecture is used to convert the RF signal to in-phase and quadrature baseband signals. The signals which are required for direct conversion are all generated within the chip by fully integrated PLLs and quadrature LO generators. The frequency of the VCO is set by internal PLL circuits, which are programmable via a 2-wire (I^2C) serial bus. The LO signals are mixed with the RF signal input and then filtered by low-pass filters to remove the upper image produced by the mixer. A variable gain amplifier is then used to adjust the baseband signal levels before processing by the channel selection filters to optimize noise performance and prevent distortion within the filters. The channel select filters are digital programmable low pass filters with 1MHz step from 4MHz to 40MHz. The output amplifier buffers the signal from the filters to increase the driving capability to the next baseband ADC.

Some innovative technique is used to correct and alleviate DC offsets inherent in direct conversion mixers, the channel select filters and output buffers.

LNA1&LNA2

LNA1 is the first LNA and receives signal from the LNB through external matching circuit, the input resistance is matched to 75 Ω coaxial cable. The LNA2 is the second LNA and is used to provide wide dynamic range, the better noise figure. The gains of both LNA1 and LNA2 are programmable by the 2-wire (I^2C) interface to insure wide dynamic range of the receiver.

AGC Amplifier

The AGC Amplifier receives the IQ signals from the quadrature mixer then amplifies them and sends to the base band low pass filter. The gain is also programmed and controlled by the 2-wire (I^2C) interface.

Baseband LPF

The bansband low-pass filter is designed to have variable cut-off frequency. The bandwidth of the LPF is selectable from 4MHz to 40MHz with 1MHz step. The DC-offset calibration can be carried out controlled by the interface. Some innovative technique ensures the filter's bandwidth variety within 5%.

Reference Oscillator

The oscillator is on-chip integrated and both the crystal and crystal oscillator are supported. 27MHz is recommended.

VCO

The receiver integrates two VCOs which ensure covering the full receiving frequency from 950MHz to 2150MHz. The VCO's bands are programmed using 2-wire (I^2C) interface. VCO1 can work from 3700MHz to 6640MHz, and VCO2 can work from 5920MHz to 9080MHz. On each VCO band, some registers are configured differently between low section and high section, in order to keep better performance flatness. After being divided by four, LO signal from 950(3800/4) MHz to 2150(8600/4) MHz can be obtained.

LO frequency	Used VCO	Divider	Note
950(3800/4)≤F≤1363(5452/4)	VCO1	4	VCO1 is used from 950 to 1579. Between the bands of below 1363MHz and upon 1364MHz, registers are fine-tuned differently.
1364(5456/4)≤F≤1579(6316/4)	VCO1	4	
1580(6320/4)≤F≤1862(7448/4)	VCO2	4	VCO2 is used from 1580 to 2150. Between the bands of below 1862MHz and upon 1863MHz, registers are fine-tuned differently.
1863(7452/4)≤F≤2150(8600/4)	VCO2	4	

PLL

The fractional-N frequency synthesizer use 27MHz reference as default. The dividers, loop filters, phase&frequency detector, charge pump are all integrated on chip.

Baseband Output Amplifier

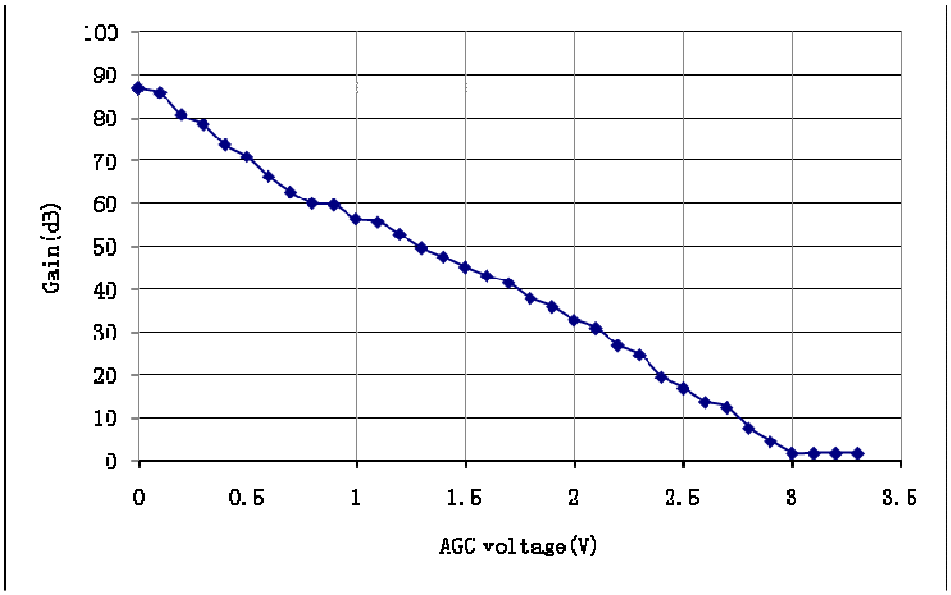
Class-AB architecture is selected for the output buffer, this makes it more flexible to the next Baseband solution's input load. The gain of this stage can also be programmed with interface to farther increase the receiver dynamic.

I^2C interface

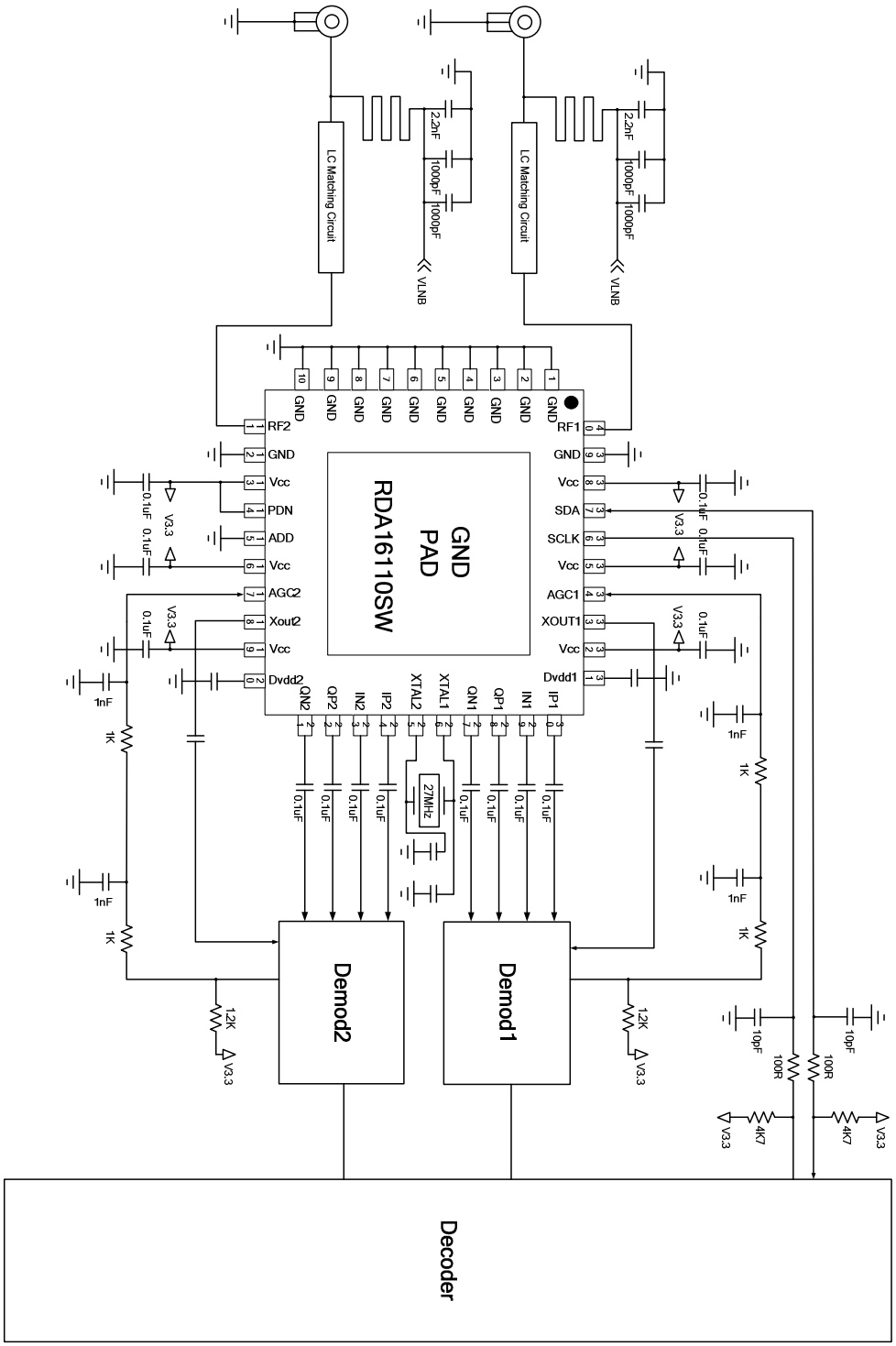
The interface is the control unit of all the analog blocks, it is provided for configuration and monitoring all internal registers, the I^2C bus consists of two wires: serial clock line (SCL) and serial data line (SDA). The LNA's gain, AGC, baseband LPF's bandwidth, VCO's and crystal oscillator's current, VCO's oscillation frequency are all controlled by the 2-wire interface.

Direct AGC control

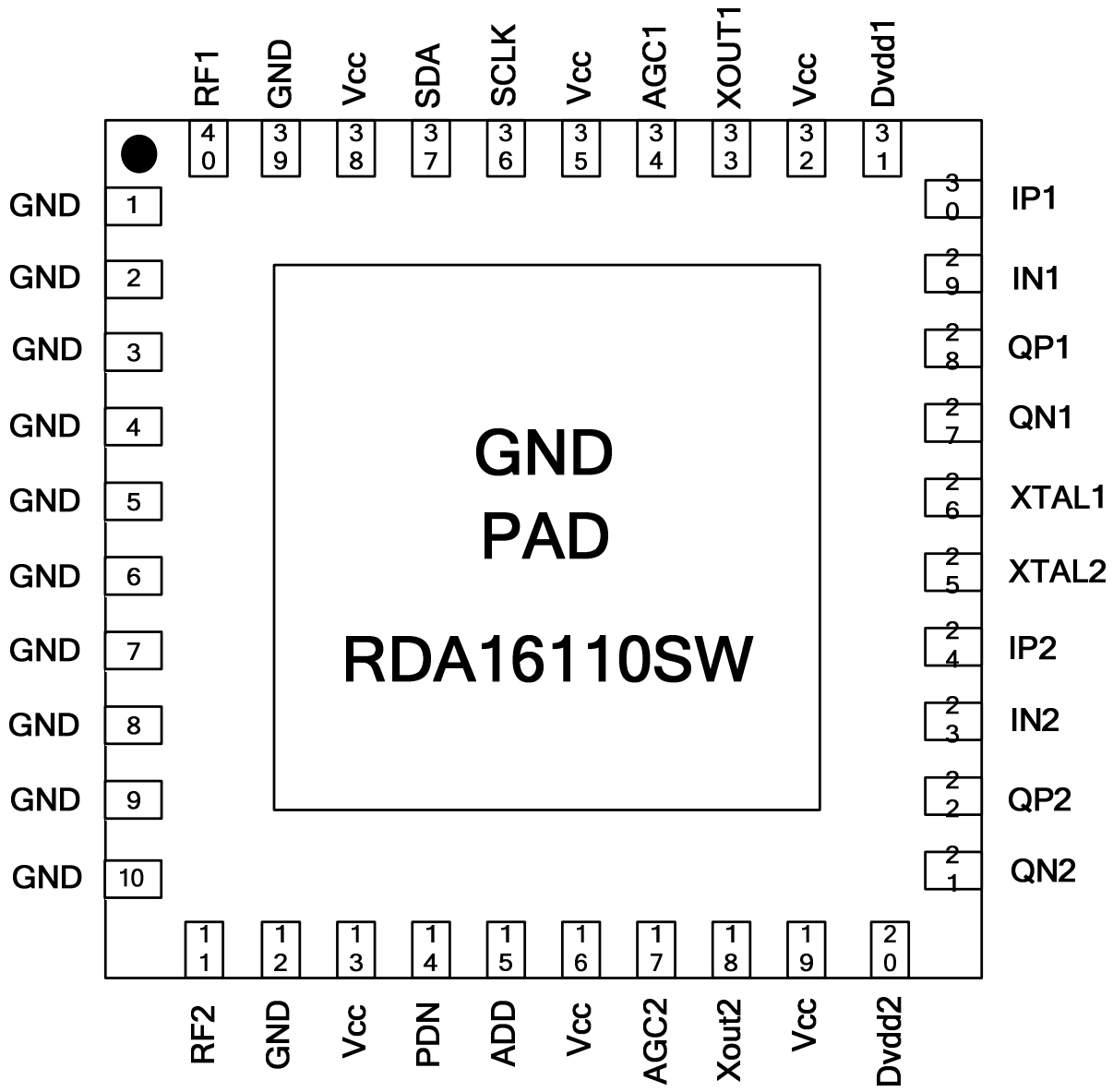
Through the AGC pin input, the receiver chain's gain can be directly controlled by the baseband solutions. The receiver gain changed inversely with the AGC control signal, this means that when AGC signal goes high, the receiver gain will drop to relevant level and vice versa.



Typical application circuit



Pin Description



Pin number	Name	I/O	DESCRIPTION
1~10,12,39	GND		Connected to Ground
11	RF2	I	The RF input pin for the channel 2
13	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
14	PDN	I	Chip power control If low, Receiver totally power down, including the crystal oscillator. If High, the chip is enabled.
15	ADD	I	I2C bus address selection terminal. Allowing the use of more than one device per I2C bus system by the voltage on this pin. See Table 8 for programming details.
16	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
17	AGC2	I	AGC control input for the channel 2
18	Xout2	O	Buffered Crystal oscillator output for demod2
19	Vcc	I	Supply voltage for Channel 2, Connected to 3.3 V
20	Dvcc2	O	Output of the supply voltage for channel2's dsp, Connected to cap
21	QN2	O	Negative Base-Band Q Channel2 Out
22	QP2	O	Positive Base-Band Q Channel2 Out
23	IP2	O	Positive Base-Band I Channel2 Out
24	IN2	O	Negative Base-Band I Channel2 Out
25	Xtal2	I/O	Connect to Crystal (27MHz is recommended)
26	Xtal1	I/O	Connect to Crystal (27MHz is recommended)
27	QN1	O	Negative Base-Band Q Channel1 Out
28	QP1	O	Positive Base-Band Q Channel1 Out
29	IN1	O	Positive Base-Band I Channel1 Out
30	IP1	O	Negative Base-Band I Channel Out
31	Dvcc1	O	Output of the supply voltage for channel1's DSP, Connected to cap
32	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
33	Xout1	O	Buffered Crystal oscillator output for demod1
34	AGC1	I	AGC control input for the channel 1
35	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
36	SCLK	I	Serial clock input
37	SDA	I/O	Serial data input/output, connected to 3.3V with 10kΩ resistor
38	Vcc	I	Supply voltage for Channel 1, Connected to 3.3 V
40	RF1	I	The RF input pin for the channel 2

Electrical Specifications

Table 1 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	AVDD	3	3.3	+3.6	V
Ambient Temperature	T_A	-25	27	+85	℃

Table 2 DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V_{IL}	0		0.3*VDD	V
CMOS High Level Input Voltage	V_{IH}	0.7*VDD		VDD	V
CMOS Threshold Voltage	V_{TH}		0.5*VDD		V

Table 3 Power consumption specification

(VDD =3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Symbol	Description	Condition	TYP	UNIT
ICC	Both Channels ON	Normal work	280	mA
ICC	One Channel ON	Normal work	145	mA
ICC	Standby mode	PDN = 1,Enable=0	6	mA
ICC	Sleep mode	PDN = 0	250	uA

Table 4 System Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	f_{IN}		900		2200	MHz
Noise Figure	NF	Max Gain (Minimum AGC)		3.5	5	dB
Input refered third-order intercept	IIP3	Minimum Gain (Maximum AGC)	9.5	10	11	dBm
Input refered econd-order intercept	IIP2	Minimum Gain (Maximum AGC)		60		dBm
Isolation of RF1 and RF2			36	45	60	dB
Gain flatness over frequency	GF	Input freq=900 to 2250MHz		4	5	dB
IQ amplitude balance	IQAB				0.5	dB
IQ phase balance	IQPB				0.5	Deg
Minimum voltage conversion gain	Gv(min)	AGCIN set to maximum (3.3 V)		-2		dB
Maximum voltage conversion gain	Gv(max)	AGCIN set to minimum (0.1V)		85		dB
Voltage conversion gain step	Gv(step)			0.2		dB
Matched input resistance	R_{IN}	After matching		75		Ω
Power up setting time	PUST			1		ms
Input reflection coefficient	S11	After matching		-10		dB

Table 5 Frequency Synthesizer Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SW}	RX Switch on time			200		us
f_{RFLO}	synthesizer frequency		900		2200	MHz
PN1	Phase noise	Δf=1kHz		-88	-80	dBc/Hz
PN2		Δf=10kHz	-100	-95	-90	dBc/Hz
PN3		Δf=100kHz	-110	-105	-100	dBc/Hz
PN4		Δf=1MHz	-138	-133	-130	dBc/Hz

Table 6 Baseband LPF and Output Amplifier Characteristics

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3 dB baseband filter bandwidth	BBF(3dB)		4		40	MHz
Cutoff frequency accuracy at -3dB	FC				+/-5	%
LPF 2fc attenuation	LPF ATT1		25			dB
Flatness	FLTN			0.5	1	dBpp
Group delay	Td(g)			2		ps
Maximum differential output voltage		Clipping level		0.9*VDD		Vpp
Output common mode voltage			0.3*VDD	0.5*VDD	0.6*VDD	V
Differential Output offset voltage				30		mV
IQ output impedance			25	45	55	Ω
Output Amplifier minimum load impedance			1K			Ω
Output Anplifier maximum Load capacitance					10	pF

Table7 XTAL Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
Differential output voltage	XTAL2		800		mVpp
	XTAL1		810		
	XOUT1		800		
	XOUT2		727		
Common mode voltage	XTAL2		0.4		V
	XTAL1		0.5		
	XOUT1		0.81		
	XOUT2		0.81		

Table 8 I^2C Address selection

ADD input voltage	I2C Address				
	bit<7:4>	bit<3>	bit<2>	bit<1>	
	0001	MA1	MA0	0	1
0 V ~ 0.1 VDD	0001	0	0	Channel_1	Channel_2
open	0001	0	1	Channel_1	Channel_2
0.9 VDD ~ VDD	0001	1	1	Channel_1	Channel_2

Table 9 XOUT1&XOUT2 description

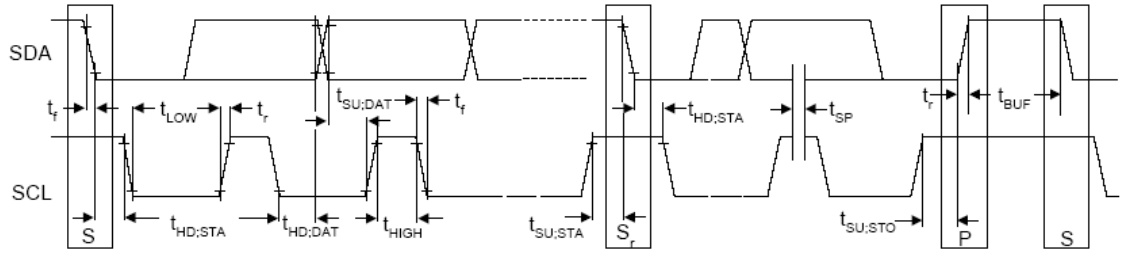
XOUT_EN1(35pin)	XOUT1(33pin)
LOW	No output
HIGH	Output XTAL(crystal) frequency

XOUT_EN2(16pin)	XOUT2(18pin)
LOW	No output
HIGH	Output XTAL(crystal) frequency

Table 10 I²C bus characteristics

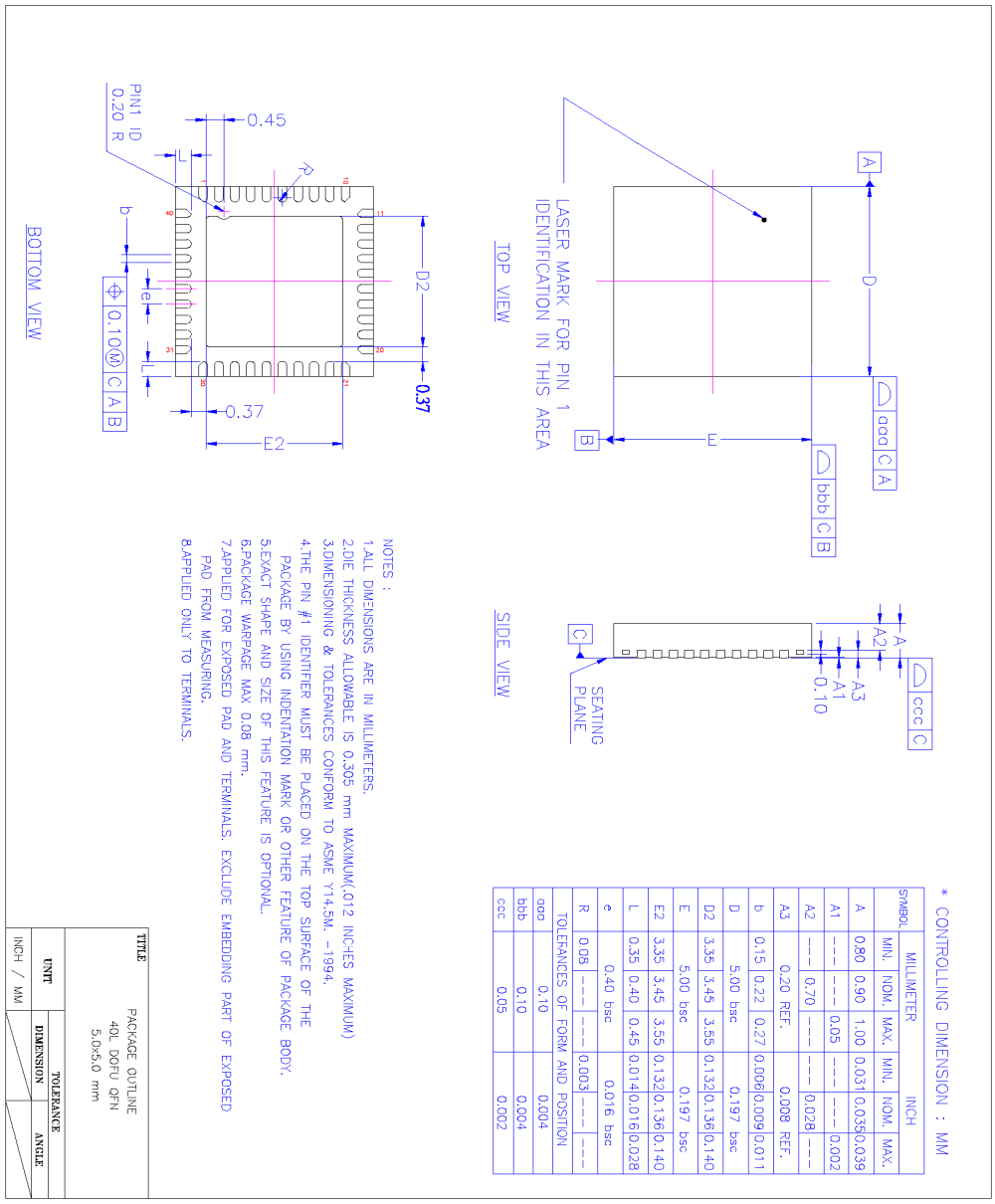
(VDD = 3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

PARAMETER	SYMBOL	Test Condition	MIN	TYP	MAX	UNIT
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			μs
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$T_{HD, STA}$		0.6			μs
LOW Period of SCL Clock	t_{LOW}		1.3			μs
HIGH Period of SCL Clock	t_{HIGH}		0.6			μs
Data Setup Time	$t_{SU,DAT}$		100			ns
Data Hold Time	$t_{HD,DAT}$		0		0.9	μs
SCL and SDA Rise and Fall Time	t_f,t_f				300	ns
Setup Time for a Repeated START Condition	$t_{SY,STA}$		0.6			μs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs
Capacitive Load for each Bus Line	C_B				400	pF



I²C Timing Diagram

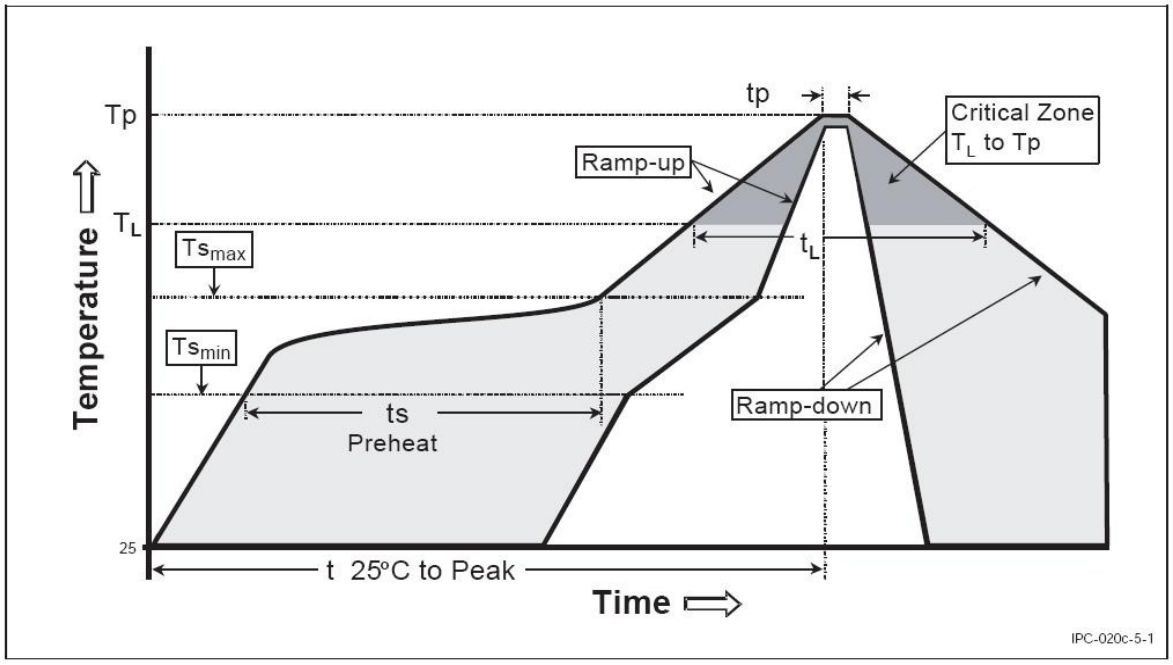
Package Outline



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	---	---	0.05	---	---	0.002
A2	---	0.70	---	---	0.028	---
A3		0.20 REF.			0.008 REF.	
b	0.15	0.22	0.27	0.006	0.009	0.011
D		5.00 bsc			0.197 bsc	
D2	3.35	3.45	3.55	0.132	0.136	0.140
E		5.00 bsc			0.197 bsc	
E2	3.35	3.45	3.55	0.132	0.136	0.140
L	0.35	0.40	0.45	0.014	0.016	0.028
e		0.40 bsc			0.016 bsc	
R	0.08	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

40-Pin 5x5 Quad Flat No-Lead (QFN)

Solder Mounting Condition



Classification Reflow Profile

Table-I Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – III Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" classification temperatures and profiles defined in Table-I II III whether or not lead free.

Table 10 Junction Temperature specification

(VDD =3 to 3.6 V, T_A = -25 to 85 ℃, unless otherwise specified)

Symbol	Description	Condition	MIN	TYP	MAX	UNIT
ΘjA	Junction to Ambient Thermal Resistance			21.6		℃/W
T_j	Junction Temperature	Ta (Ambient Temperature) -25 ℃	-7	-5.5	-4	℃
T_j	Junction Temperature	Ta (Ambient Temperature) 25 ℃	43	44.5	46	℃
T_j	Junction Temperature	Ta (Ambient Temperature) 85 ℃	103	104.5	106	℃

Note: Tj = Ta +ΘjA * Power Consumption, MIN value comes from 3.0v VDD, TYP value comes from 3.3v VDD, MAX value comes from 3.6v VDD.

Table 11 Absolute Maximum ratings

Symbol	Description	MIN	MAX	UNIT
VDD	Power supply voltage	-0.3	3.6	V
T_{oper}	Operating ambient Temperature	-25	85	℃
T_j	Junction Temperature		125	℃

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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